



Electrical characterization & TEM study of the physical mechanism simplified in reliability issues of Ge-rich GST phase-change memories

Martin Coue

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THÈSE

Pour obtenir le grade de

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préparée au sein du **CEA Leti**
dans l'**École Doctorale Electronique, Electrotechnique,**
Automatique et Traitement du Signal

Caractérisation électrique et étude TEM des problèmes de fiabilité dans les mémoires à changement de phase enrichis en germanium

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Introduction

Since the invention of the first electronic computers by Alan Turing in 1937 [Turing 1937], the importance of memories in our daily life hasn't stopped to rise. Nowadays they can be found in a vast range of electronic systems such as personal computers, laptops, cellphones, televisions, appliances, and many others. As the applications of these memories have grown more and more various, different kind of technologies have been developed to answer specific needs. In particular, the development of embedded nonvolatile memories (eNVMs) has become a major need for the industry as the market of autonomous, decentralized and mobile units has risen up during the last decade. If flash technology has been dominating the market until now, its limitations have been reached, opening the way to a new era for non-volatile memories. Thanks to their scalability, endurance, write performances and low cost per bit when compared to other eNVMs, Phase Change Memories (PCMs or PRAMs) are often seen as one of the most promising technology to completely re-think the design of the memory subsystem, allowing to gain orders of magnitude improvements in speed and/or power consumption and to improve the memory hierarchy gap (as storage-class memory between the CPU and hard-disk). Moreover, PCMs offer great potential for low density embedded memories (to be integrated in microcontrollers and Systems on Chip (SoC)). Finally, exciting new applications and markets can be addressed, as new functionalities coupled with logic circuits to enable block power-down (in the Internet-of-Thing "Normally-Off" applications), or use as artificial synapses in neuromorphic systems for Big-Data analytics. However, some requirements still need to be fulfilled, in particular concerning the reliability of the memories when exposed to high temperatures. During the last few years, many efforts have been made to improve the thermal stability of PCMs, and notable progress has been achieved in this way by experimenting innovative materials such as germanium-enriched $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (Ge-rich GST). Unfortunately this solution raises another issue, which is the drift of the resistance over time. This phenomenon, already observed and studied in $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) and other phase change materials was especially known to increase the resistance of the RESET state, but has been proven recently to have also an impact on the SET state of Ge-rich GST devices. In this thesis, we have investigated physical mechanisms governing Reliability of Ge-rich Phase-Change Memories by means of intensive electrical characterization & TEM analyses.

Phase-Change Memories

In the following chapter we will present the context of this work with a rapid overview of the semiconductor memory market and a comparison of emerging non-volatile memories. We will then focus on the PCM technology, introducing its working principle, its advantages, and its drawbacks. The main structures of PCM cells will be detailed before going into the physics of crystallization in phase-change materials. The goals and outline of this thesis will be given after presenting the main topic of our studies, namely the reliability issues of Phase-Change Memories (PCM), with the description of the mechanisms responsible for the loss of data.

1.1 Context

1.1.1 The semiconductor memory market

Since the invention of the first transistor by Bell Labs (USA) in 1947, the market of Integrated Circuits (IC) has impressively soared, and the total revenue now exceeds 300 billion dollars (fig.1.1).

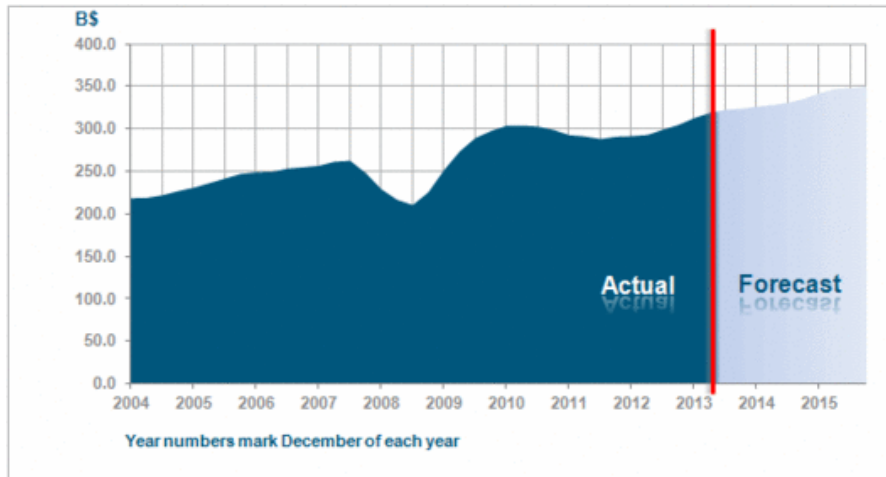


Figure 1.1: Worldwide semiconductor industry revenue, data from WSTS [Statistics 2013]

The semiconductor (SC) memory market represents a consistent share of the IC market, with approximately \$82B of revenues in 2013 (1/4 of IC revenues) [De Charentenay 2015]. It is divided into two main categories depending on the type of system in which the memories are integrated. Fig.1.2 shows some application fields for both categories: *stand-alone* memories are mainly dedicated to data

storage and main RAM memories of computers, servers, cellphones, video game consoles or tablets; *embedded* memories regroup all applications where the memory device is co-integrated with the CMOS elements on the same chip (System on Chip or SoC), like microcontrollers (MCUs) for the automotive and industrial fields, smart-cards (SIM cards, ID cards...), mobile Micro Processor Units (MPUs) for cellphones, and other general electronic purposes like appliances or toys.

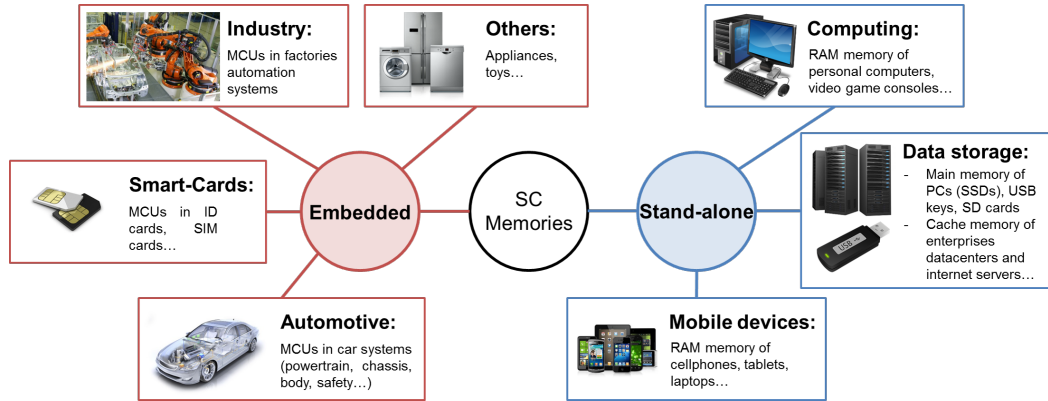


Figure 1.2: Stand-alone and embedded applications of semiconductor memories.

The distribution of the SC market revenues is detailed in fig. 1.3, with \$67B for stand-alone applications and \$15B for embedded systems. Flash and DRAM share most of the stand-alone sales with respectively 43% and 53% of the revenues in 2013 while SRAM is the most represented technology in embedded systems with 73% of the embedded market revenues.

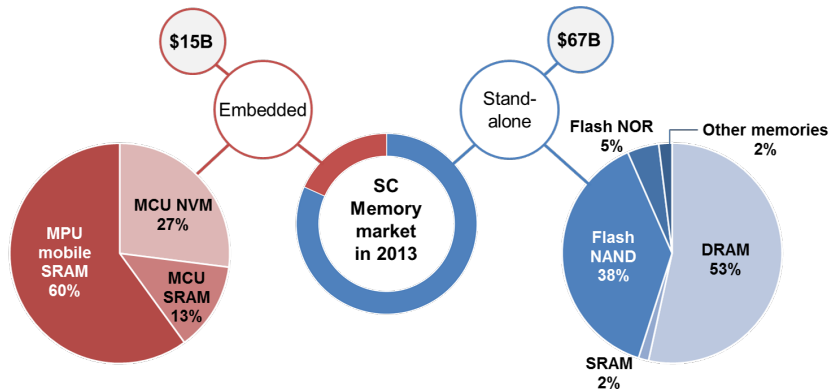


Figure 1.3: The semiconductor memory market in 2013.

1.1.2 Introduction to non-volatile memories

Random-Access Memory The role of Random-Access Memory (RAM) in modern computers is of primary importance. It is used to store temporarily all the data (text, images...) and software (word processors, web browsers, video games...)

which are in use, as well as a part of the Operating System (DOS, Windows, Mac OS, Linux...). For example, when the user opens a software (originally installed and stored on the hard drive), the computer stores it temporarily in the RAM memory, faster to access than the hard drive. In this case, Random-Access Memory thus enables a much faster communication between the Central Processing Unit (CPU) - the heart of the computer which processes the data - and the software being used. Such a memory must therefore provide very low accessing times and a high reliability to ensure a proper user experience.

Two types of Random Access Memories Random-Access Memories are divided into 2 categories: volatile and non-volatile. Volatile memories like Static RAM (SRAM) and Dynamic RAM (DRAM) Data stored in volatile memories will be lost once power is switched off while non-volatile memories (NVMs) can keep the information even without any power source.

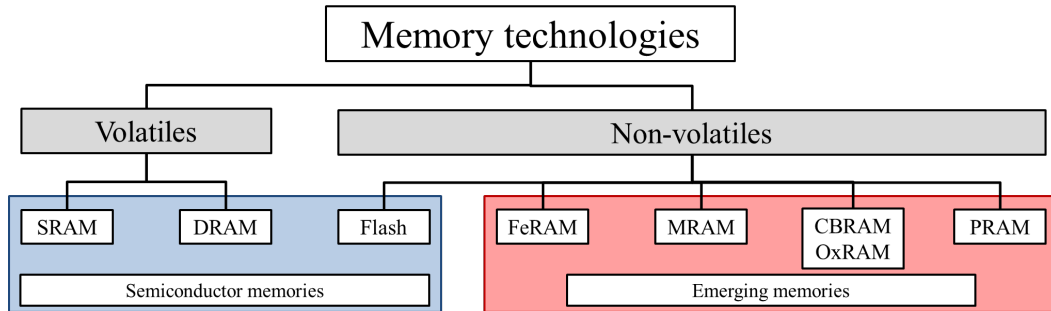


Figure 1.4: Organization chart of the main memory technologies. [Natarajan 2009]

Figure 1.4 shows an organization chart of the main memory technologies (including technologies already on the market and others that are currently under development). While the volatile Dynamic and Static RAMs (respectively DRAM and SRAM) have been dominating the field of RAM memories for decades since the 60's, new types of non-volatile RAMs have risen up during the last twenty years, especially flash memory which has become the new dominant technology on the market. Besides DRAM, SRAM and flash, new alternatives are being explored, representing the so-called emerging memories technologies.

1.1.3 Focus on Flash non-volatile memory technologies and market

Flash technology: the floating gate transistor To store data, a flash memory cell uses a MOSFET transistor in which a floating gate (typically made of polycrystalline silicon) is inserted in-between the control gate and the MOSFET channel. This floating gate is electrically isolated from the rest of the device by two insulating layers, namely the control oxide and the tunnel oxide (fig.1.5).

In this type of memory the information is stored by transferring electrons in or out of the floating gate, which modifies the threshold voltage of the MOSFET and enables the creation of two distinct states (binary 1 or 0).

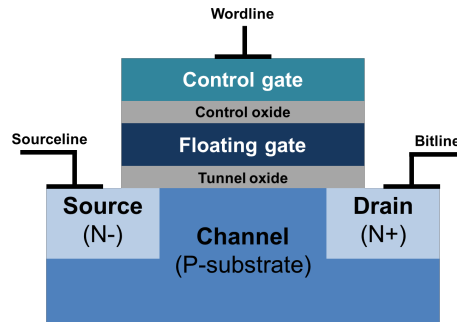


Figure 1.5: Schematic of a floating gate transistor used in flash technology.

Flash memories are divided in two different groups depending on the cells arrangement in the memory arrays:

- the NOR architecture in which cells are connected in parallel (fig.1.6), enabling to access each individual cell separately. NOR devices are mainly used for instruction codes storage in operating systems of cellphones, motherboard or microcontrollers.
- the NAND architecture in which cells are connected in series (fig.1.6), which forbids the access to individual cells but enables to store a high volume of data. NAND flash is the main technology used in USB storage devices as well as most memory card formats and solid-state drives available today.

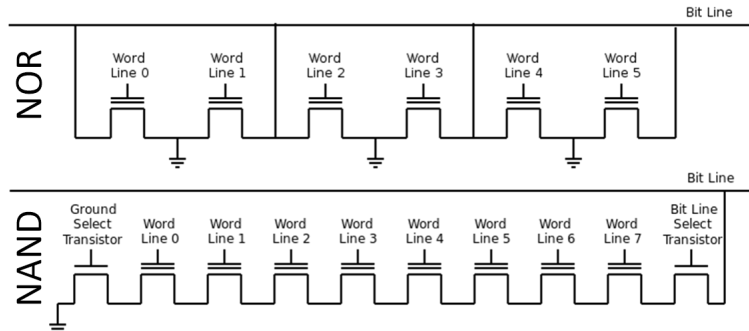


Figure 1.6: The NOR and NAND architectures of Flash memories.

The simplicity of Flash structure makes it a highly scalable technology, but the two architectures do not require the same space for each cell: while one cell occupies an area of $4F^2$ in the NAND architecture, this value rises to $10F^2$ in the NOR one, even when using exactly the same semiconductor device fabrication because NOR Flash cells require a separate metal contact for the drain of each cell.

Stand-alone memory applications The stand-alone memory market is currently dominated by 5 integrated device manufacturers (Samsung, Micron, SK

Hynix, Toshiba and SanDisk) which share 95% of the overall revenues in 2013 (fig.1.7). If we focus on non-volatile memories, Flash represents approximately 95% of global NVMs sales for stand-alone applications, driven by the expansion of NAND memory over the past few years.

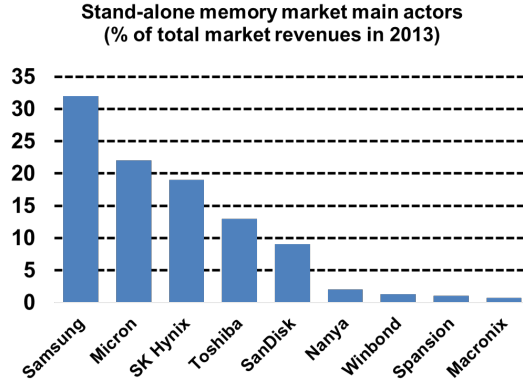


Figure 1.7: Main actors of the stand-alone memory market (reproduced from [Tortorelli 2015]).

As NAND memory is mainly dedicated to store a large amount of data, user data storage is thus the main market aimed by this technology typically found in USB keys, memory cards, cellphones, tablets and most recently in Solid-State Disks (SSD). Fig.1.8 shows a analysis of the NAND market evolution between 2010 and 2014 [Choi 2014]. The explosion of the mobile devices market, coupled to the progressive replacement of Hard Drive Disks (HDDs) by Solid-State Disks (SSDs) are two of the main reasons why NAND rules over the NVM market for stand-alone applications.

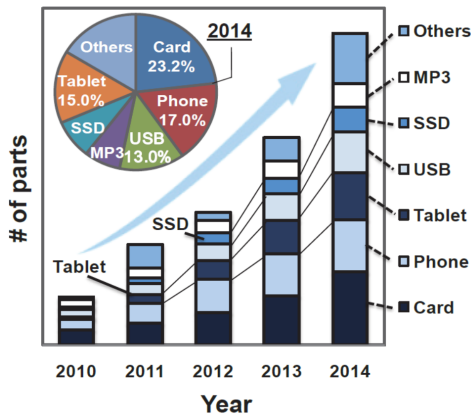


Figure 1.8: Analysis of the NAND market evolution between 2010 and 2014 (reproduced from [Choi 2014]).

This rise has been made possible essentially by the cost diminution of NAND memories with the reduction of cells size thanks to the improvements of lithography techniques. From 1998 to 2012 the size of a NAND cell has been indeed divided by 1000 [Burr 2013], leading to a radical decrease of NAND cost from approximately \$10k/GBit in 1995 to \$0.05/GBit in 2015 [De Charentenay 2015].

Embedded applications Concerning embedded memories, we will focus on the MCU market since it is the main field of applications for embedded non-volatile memories (eNVMs). This market is less concentrated than the stand-alone memory market with the top ten producers being large semiconductor IC manufacturers (fig.1.9).

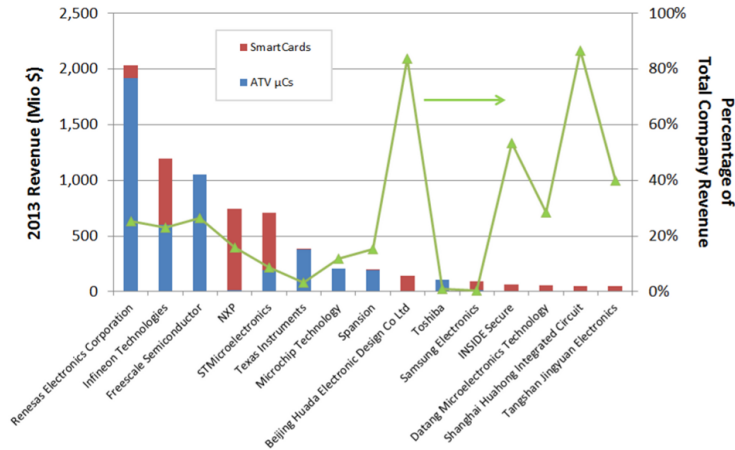


Figure 1.9: Main actors of the MCU market (automotive & Smartcards) [Strenz 2014].

Fig.1.10 compares the evolution of market size for stand-alone Flash (NAND and NOR) and MCUs [Baker 2012]. Although NAND Flash still represents the most rapidly growing market, MCU sales are also growing steadily and are expected to reach \$20B by the end of the year 2015.

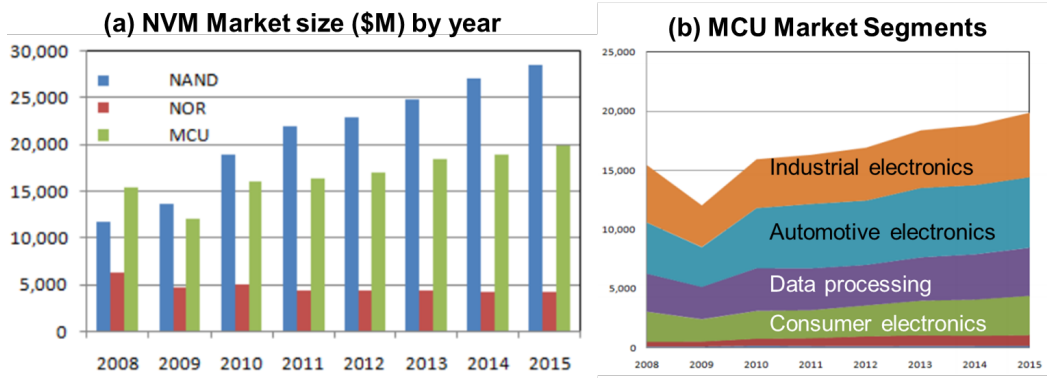


Figure 1.10: The evolution of the MCU market from 2008 to 2015 (reproduced from [Baker 2012]).

Embedded NVMs are currently estimated to represent 50% of the MCU market, with expectations to see this number rising up in the next years [Niegel 2011], making this field a strong driver for eNVM innovations.

MCUs are used in a wide variety of applications, with very special specifications for each of them. Fig.1.11 displays the main criteria that eNVMs must fulfill to address each application [Baker 2012].

Market	Fast Code Execution	Robust/ZD Quality	Pgm/Erase Endurance	Read/Pgm/ Erase Pwr	Sector Size P/E Time
Auto P-Train & Chassis	3-5 High compute power req	5 Mission- and safety-critical	4 Increasing EE Emul Requirement	3 Self-heating, Perf. tradeoff	2 Cost of boot blocks, Factory Pgm.
Auto Body	2 Moderate compute power	5 Mission- and safety-critical	3 Increasing EE Emul Requirement	4 Many always-on devices	3 Cost of boot blocks, etc.
Industrial Control	3-5 High compute power req	3 Also control critical functions	2 Moderate EE Emulation Req.	4 Many apps are low power	3 Cost of boot blocks
Portable & Consumer	2 Moderate for many apps	2 Shorter lifetimes, less critical	2 Moderate EE Emulation Req.	4 Many apps are low power	3 Cost of boot blocks
Smart Cards	2 Less important than pwr, etc	2 Shorter lifetimes in many cases	5 EE function with frequent updates	5 Critical for contactless, etc	5 Also important for contactless, etc

Figure 1.11: Requirements for each eNVM application with relative importance (max = 5, min = 1) [Baker 2012].

Since a single technology cannot answer all these needs, different types of Flash architectures have been developed:

- the 1T-NOR architecture where a single floating-gate transistor is used to store data
- the 2T-NOR (or EEPROM) where 2 transistors are used in series
- the 1.5T Flash (or split-gate) in which the control gate only covers part of the tunnel oxide and floating gate

The main applications, advantages and drawbacks of these technologies are summarized in fig.1.12.

1.1.4 Limits of Flash technology and solutions

As said above, Flash technology is based on floating gate transistors: to reduce the size of a Flash cell it is thus necessary to shrink the dimensions of the oxides layer surrounding the floating gate. But this shrinking will soon reach its limits as physical issues start to appear when the tunnel oxide is too thin: there is indeed a threshold value for the oxide thickness below which the electrons can escape the floating gate because of quantum tunnelling effects. Scaling down the tunnel oxide also affects the endurance of the cell: as the electric field applied to the device gets stronger and stronger with smaller dimensions, more defects appear in the oxide layer, fostering

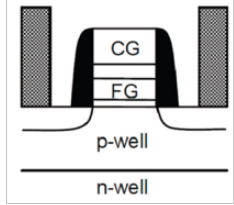
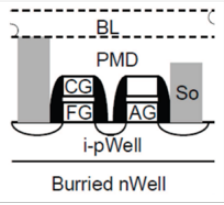
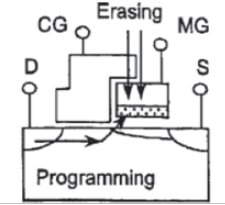
	1T	2T	Split-gate
			
Applications	Automotive	User data storage	Various
Advantages	High reliability, small dimensions	Low power consumption	Speed, reliability, low power
Drawbacks	High tension, high current, low speed	High tension, big dimensions	Complexity of fabrication

Figure 1.12: Main Flash architectures used in embedded applications [Strenz 2011].

the electrons leakage from the floating gate. Another important issue when scaling down Flash memories lays in the increase of interference between neighboring cells. A capacitive coupling can indeed appear because of the modification of the transistor's threshold voltage implied by the charge stored in a neighboring cell. It is thus necessary to keep a certain distance between the cells to ensure the reliability of the devices. At last, shrinking the dimensions of the floating gate transistor implies that fewer electrons can be stored in the floating gate. This leads to another issue, as reliability problems start to appear when dimensions do not enable more than 10 electrons to be stored, so that quantum effects must be taken into account.

As these intrinsic physical limits cannot be avoided with the current materials and architectures used in Flash fabrication, other solutions are considered to increase its density. Some studies are currently focusing on new materials with better performances for the floating gate, like silicon nitride (SiN) or nanocrystals which lower the leakage of charges towards the tunnel oxide. The control oxide could also be replaced by high permittivity materials (or "high k materials") like HfO₂, ZrO₂ or AlO₃, which ensure a good coupling between the control gate and the floating gate while limiting the leakage current. At last, electrostatic interference between neighboring cells can be lowered by using low permittivity materials (SiO₂, SiOCH...) to separate each transistor.

Besides these researches for alternative materials, new types of architectures have also been considered to further decrease the cost of Flash memories. As opposed to the currently adopted planar structures, three-dimensional architectures have been introduced: one approach, called the stacked architecture, consists in several layers of classical planar memories which are interconnected by metallic junctions [Jung 2006]. In other architectures like BiCS [Tanaka 2007], TCAT [Jang 2009], VSAT [Kim 2009] or VG-NAND [Lue 2010], the transistor channel and the gate form crossed 3D structures as depicted in fig.1.13.

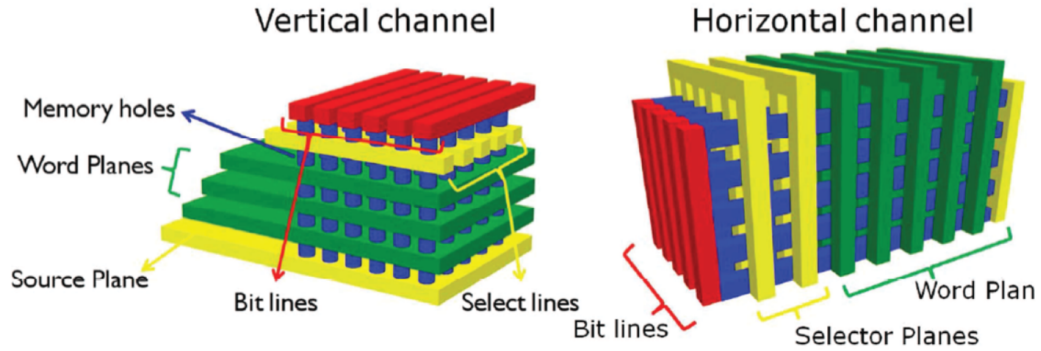


Figure 1.13: Schematic of 3D Flash architectures with vertical transistor channels (left) or horizontal (right) [Arreghini 2013].

1.2 Emerging non-volatile memories

In order to overcome the limits of current technologies (in terms of scaling, performance or cost), several new technologies have been intensively studied in the last decades. Their working principles, main characteristics and application fields are briefly reviewed in the next paragraphs.

Ferroelectric RAM (FeRAM) This type of RAM exploits the two stable polarization states of a ferroelectric material (typically lead zirconate titanate $\text{Pb}(\text{Zr}, \text{Ti})\text{O}_3$ or PZT) which naturally contains electric dipoles, because of the distribution of anions and cations inside its structure. The application of an electrical field to the material enables to change its polarization state durably, and thus to program the device in two distinct states (fig.1.14). The 1T-1C (one transistor and one capacitor) storage cell design in an FeRAM is similar in construction to the storage cell in widely used DRAM since both cell types include one capacitor and one access transistor. In a DRAM cell capacitor, a linear dielectric is used, whereas in an FeRAM cell capacitor the dielectric structure includes ferroelectric material.

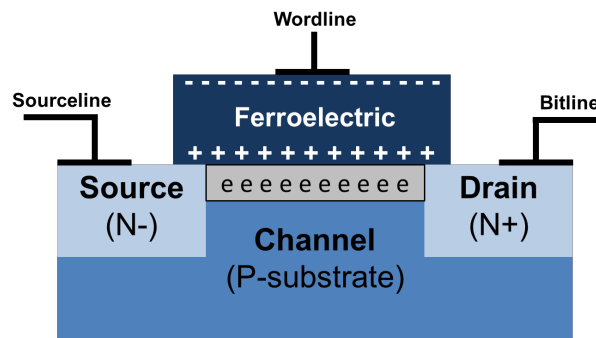


Figure 1.14: Schematic of a FeRAM cell.

To read the information, the cell is set to its "0" polarization state. If this implies a change of polarization, a charge variation is measured, meaning that the cell was in

its state "1". If no variation is measured, then the cell was in a state "0". This means that the reading step in a FeRAM cell is a destructive process. The advantages of this technology over Flash are its lower power consumption, faster write performance and greater number of write-erase cycles. But the working principle of FeRAM implies that the information stored in one cell is lost after reading, because the cell has to be put back in its "0" state, because of its lower density (thus higher cost), its small scaling potential and the difficulties usually encountered during the integration of the devices, FeRAM is generally not considered as a future alternative to Flash memories at this date.

Magnetic RAM (MRAM) MRAMs can be seen as the magnetic version of FeRAMs as they use the two stable *magnetic* states of a ferromagnetic material. An MRAM cell is made of two ferromagnetic plates which can both hold a magnetization, separated by a thin insulating layer (fig.1.15). One of the two plates is a permanent magnet set to a particular polarity while the other plate's polarity can be changed by the means of an external magnetic field applied to the cell. This change of polarity induces a change of the cell's resistance, and thus enables the distinction between two resistive states, making it suitable for memory applications.

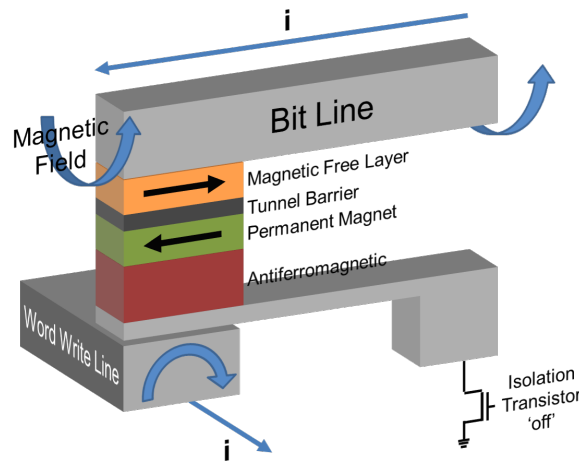


Figure 1.15: Schematic of a classic MRAM cell.

The main drawback of this technology comes from the many different layers needed for its fabrication, using multiple materials which are not usual in the microelectronic field, making it difficult to integrate in the production lines of current microelectronic manufacturers. Moreover the first generation of MRAMs had a limited scaling potential, with high currents needed for the programming and a small resistance window between the two resistive states. More recently, the Spin-Transfer Torque MRAMs (STT-MRAM) technology has been introduced, in which the orientation of the free magnetic layer is modified using a spin-polarized current rather than an external magnetic field. Thanks to this new technique, STT-MRAMs could theoretically reach similar performances than SRAM with densities close to DRAM

but much lower power consumption than the latter, and an unlimited lifetime since no electronic nor material movement is engaged.

Resistive RAMs (RRAMs): Oxide Resistive RAM (OxRRAM) & Conductive-Bridging RAM (CBRAM) OxRRAM and CBRAM technologies are both based on the reversible change of resistance inside an active material by the creation and destruction of a conductive filament between the two electrodes (fig.1.16).

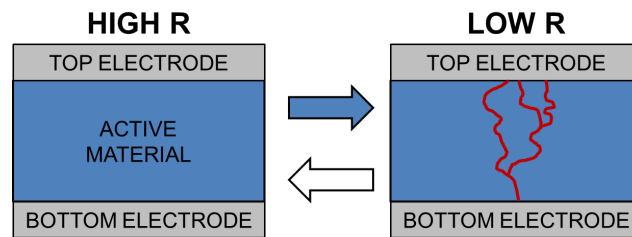


Figure 1.16: Schematic of the working principle of CBRAM/OxRRAM device. The application of an electrical pulse to the cell enables the reversible creation of a conductive filament inside the active material (typically GeS_2 or GdO_x in CBRAMs, and HfO_2 or TiO_2 in OxRRAMs).

In the case of CBRAM, the active material is a solid electrolyte (e.g. GeS_2 or GdO_x for example) surrounded by two solid metal electrodes. One of these electrode is inert (e.g. platinum or tungsten) while the other one is electrochemically active (e.g. copper or silver), leading to redox reactions with the active material when a voltage or current pulse is applied to the cell, and thus to the creation (or destruction) of a conductive filament.

In an OxRRAM cell, the active material is usually a very thin layer (a few nanometers) made of a transition metal oxide (e.g. HfO_2 or TiO_2). In its initial state, the oxide layer is insulating, and a first electrical stress is needed to make it conductive (the so-called "forming" step). The reversible switching between the high and low resistance states is then induced by the application of an electrical pulse to the cell, creating (or erasing) a conductive filament which is thought to be made of oxygen vacancies [Waser 2009].

It should be said that for both technologies, the physics implied in the formation and destruction of the conductive filament is not totally understood at this date and still being discussed.

When compared to Flash memory, CBRAM and OxRRAM exhibit faster write times, higher endurance and lower power consumption. Moreover these technologies theoretically need only a few ion widths to work, making them scalable to sizes much smaller than Flash. Their integration in the Back-End-Of-Line is also much simpler, leading to simpler construction and lower costs. But because of the great variability of the cells performances, and because we still don't have a full understanding of the physics involved in their working process, these technologies are still not enough mature to be brought to the market.

Phase-Change RAM (PRAM) Phase-Change RAMs (also known as PCM, PCRAM, Ovonic Unified Memory, Chalcogenide RAM or C-RAM) use the two resistive states of a chalcogenide material to store data. As this technology is the main interest of this work, its working principle and other characteristics will be detailed throughout the next sections and chapters.

Finally, the main characteristics, advantages and drawbacks of the emerging technologies introduced above are summed up in table 1.1 [Tortorelli 2015].

Table 1.1: Main characteristics, advantages and drawbacks of emerging NVMs [Tortorelli 2015].

	FeRAM	MRAM	CBRAM	OxRRAM
Maturity	High	Medium	Low	Low
Scaling potential	Low	Medium	Unknown	High
Cell surface	20 F ²	6 F ² - 40 F ²	4 F ²	4 F ²
Speed	High	High	Medium	Medium
Data retention	Good	Medium	Unknown	Unknown
Endurance	High	High	Medium	Medium
Power consumption	Low	Variable	Low	Low
Integration ease	Medium	Low	High	High
Cost	High	High	Unknown	Unknown
Drawbacks	Destructive reading, scaling	Integration, scaling	Variability, under-standing	Variability, under-standing

1.3 History of Phase-Change Memories

1.3.1 The beginning of Random Access Memories

The basic principles of electronic computers as we know them today were first stated by Alan Turing in 1937 [Turing 1937]. The functionality of this new kind of technology relied on a form of memory to store all the information and data needed, and so were created paper punched cards used in the very first computer devices. The limits of this technique were however quickly reached, and Turing pointed out the need of new types of memories to allow the full development of computers [Turing 1947]. Magnetic core memories were invented a few years later and used as the main memory of the first commercialized electronic computers, but the real revolution started in the late 60's with the rise of solid state memories. This new era gave birth to Random Access Memories (RAM) such as Static RAM (SRAM) and Dynamic RAM (DRAM), more practical and much denser than magnetic core memories. But

unlike the latter, SRAM and DRAM are both volatile, meaning they lose all the information they have been storing once power is turned off. Further research was therefore needed to develop a new kind of solid state memory with a density similar to SRAM and DRAM, but non-volatile, and here was the opportunity for Phase Change RAMs to make their first appearance on the memory stage.

1.3.2 Birth of Phase-Change Memories

The idea of using the peculiar behaviors of phase-change materials to make solid state memories was already explored since the early 60's: the first patent on the subject was filled in 1961 by Dewald, Northover and Pearson, who developed the idea of "multiple resistance semiconductor elements" [Dewald 1966]. In their patent they describe the main operations of a two-terminal device "capable of operating in two resistance states", i.e. a low resistance state (LRS or SET) and a high one (HRS or RESET). They also mention a *threshold* value of the voltage applied to the cell "for changing the resistance state of [the device] from a first discrete high resistance state to a second discrete low resistance state". These concepts are still applicable to modern phase-change memories (PCM), but the real breakthrough in PCM history came from the work of Stanford Ovshinsky, considered as the father of PCM. Since 1960 Ovshinsky had been working on chalcogenides which are compounds or alloys containing at least one element from column VI of the periodic table, and first published his findings in 1968 [Ovshinsky 1968]. In this paper he reports the functionality of memory devices integrating an alloy of tellurium, arsenic, silicon and germanium, demonstrating the possibility to switch multiple devices continuously over a period of many months, which was a first at the time. This ground-breaking demonstration and the interest it drew from industrials constitute the real starting point of PCMs development.

1.3.3 Hibernation

In the 70's, other research teams started to work on their own PCM devices: in 1970, R. G. Neale, D. L. Nelson (both from Energy Conversion Devices) and G. E. Moore (Intel) developed the first 256-bit PCM array. But unfortunately the expansion of PCM technology quickly had to face some technical limitations. Back in 1970, the minimum feature size which could be printed on integrated circuit was about 10 μm . With this geometry, the volume of phase-change material needed to be switched was too large, resulting in huge power consumption: the cells of Neale et al. required 5 μs , 200 mA at 25 V bias to RESET the device and 10 ms, 5 mA at 25 V bias for the SET operation, consuming much more energy than other competitive memories at the time. Because of this inferiority in power efficiency the 256-bit array was never commercialized, and interest in PCMs took a step back.

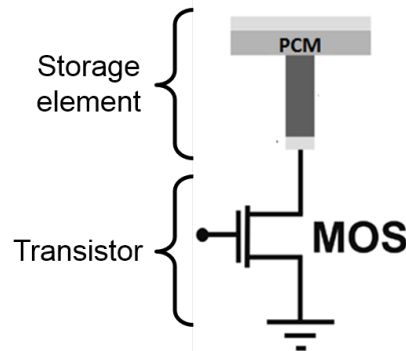


Figure 1.17: Schematic of a 1T1R PCM device.

1.3.4 Rebirth

Two decades later, in 1990, the first rewritable CD based on chalcogenides was commercialized by PANASONIC, following the discovery of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) which still remains the most studied phase-change material to date. The interest in phase-change materials quickly rose up again, and 9 years later, when the lithographic technics reached the 180 nm node and that the power needed to switch the devices seemed reasonable, the Ovonyx joint venture was created by Tyler Lowrey and Ward Parkinson along with Energy Conversion Devices, the company created by Ovshinsky in 1960, to commercialize phase-change memories. Things started to accelerate: in February 2000, just one year after the creation of Ovonyx, a license agreement was found with Intel which started to invest in the PCM technology. Ten months later, another agreement was found with STMicroelectronics, announcing the imminent commercialization of the first PCM devices, and the beginning of the modern era for PCM technology.

The main events in the history of phase change memories are listed in the table 1.2:

1.4 Working Principle of a PCM device

1.4.1 Structure and operation of a PCM device

A PCM device is divided into two main parts (fig.1.17): the storage element in which data is stored and the access transistor which enables to program or read the device. Those devices are often referred to as 1T1R devices (one transistor, one resistive element), as opposed to 1R devices which don't integrate any transistor and which are usually dedicated to research purposes where it is not needed to work on a full array of memories.

The structure of the storage element in a typical PCM cell is very simple: it is a two-terminal device consisting in two electrodes (bottom & top) enclosing a heater and a layer of chalcogenide glass (fig.1.18).

Chalcogenide glasses are materials containing one or more chalcogenide elements

Table 1.2: main events of Phase-Change Memories history.

Year	Event
1966	First patent on PCM technology granted to Dewald et al.
1968	Ovshinsky publishes his findings on phase change threshold switching
1970	First 256-bit PCM array by Neale et al.
1990	First R/W phase change CD
1999	Ovonyx joint venture is formed to commercialize PCM technology
2000	Intel invests in Ovonyx and licenses its technology STMicroelectronics also licenses the technology from Ovonyx
2002	Macronix files a patent application for transistor-less PCM
2003	Samsung begins work on PCM technology
2003-05	PCM-related patent applications filed by Toshiba, Hitachi, Macronix, Renesas, Elpida, Sony, Matsushita, Mitsubishi, Infineon and more
2004	Samsung announces successful 64 Mbit PCM array
2005	Samsung announces successful 256 Mbit PCM array, touts 400 μA programming current [Samsung 2005]
2005	Intel increases investment in Ovonyx
2005	Hitachi and Renesas announce 1.5 V PCM with 100 μA programming current [Hitachi 2005]
2005	Samsung licenses PCM technology from Ovonyx
2006	BAE Systems begins selling the first commercial PCM chip [Purvis 2006]
2006	Samsung announces 512 Mbit PCM device [EETimes 2006]
2006	Intel and STMicroelectronics show a 128 Mbit PCM chip
2007	Hynix begins pursuing PCM by licensing Ovonyx' technology
2008	Intel and STMicroelectronics announce four-state MLC PCM [Greene 2008] and begin shipping samples to customers.
2008	Numonyx announces mass production 128 Mbit PCM device to selected customer
2009	Samsung announces mass production start of 512 Mbit PCM device
2009	Numonyx announces 1 Gb 45 nm product [Numonyx 2009]
2010	Samsung releases 512Mbit PCM with 65 nm process, in Multi-Chip-Package [Krishnamurthy 2011]
2011	Samsung presented 58 nm 1.8V 1Gb PCM [Chung 2011]
2012	Samsung presented 20 nm 1.8V 8Gb PCM
2012	Micron announces availability of Phase-Change Memory for mobile devices - the first PCM solution in volume production [Krishnamurthy 2012]

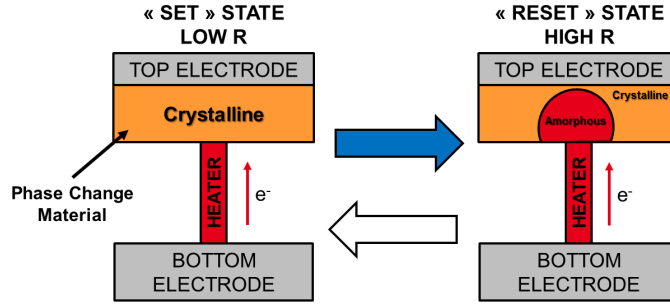


Figure 1.18: Schematic of the working principle of a PCM device. The reversible transition from the low resistance crystalline state (SET state, bit 0, left of the picture) to the high resistance amorphous state (RESET state, bit 1, right of the picture) is thermally induced by the application of a current pulse to the phase-change material through a resistive heater.

(elements from column VI of the periodic table excluding oxygen) and their unique properties are at the heart of the PCM technology. The operation of a PCM device relies indeed on the large resistivity contrast (typically 3 orders of magnitude) between the amorphous and crystalline phases of these materials to store data, i.e. bits 0 or 1. The cell can thus operate in two states depending on the chalcogenide state:

- the amorphous, high resistance state represents a binary 0;
- the crystalline, low resistance state represents a binary 1.

The device structure described in fig.1.18 is called the lance-type structure. Other PCM structures exist and will be discussed later in this chapter, but most of them derive from the lance-type one, which is the most straightforward to fabricate. In such a device the role of the heater is to enable a good heat confinement and provide an efficient joule heating of the phase-change material to fulfill the low power/energy requirements. It must then dissipate a large power and be able to sustain a large temperature gradient, so materials with high electrical resistivity and low thermal conductivity are required (titanium, tungsten, silicon and nitrogen are typically used). Clearly the choice of the phase-change material has a crucial impact on the memory performances since it will define the intrinsic limits of the device, but the structure and the scaling of the cells also have an important role to play. Indeed, shrinking the dimensions of the cell, and especially the contact area between the heater and the chalcogenide layer, can drastically change the performances of the device, in particular its power consumption. These parameters will be detailed in the next chapter when we will focus on the different ways to optimize a phase-change memory.

1.4.2 Phase-change transitions

What makes the PCM technology interesting is that the transition between the crystalline and amorphous phases (fig.1.19) is reversible, thermally-induced and there-

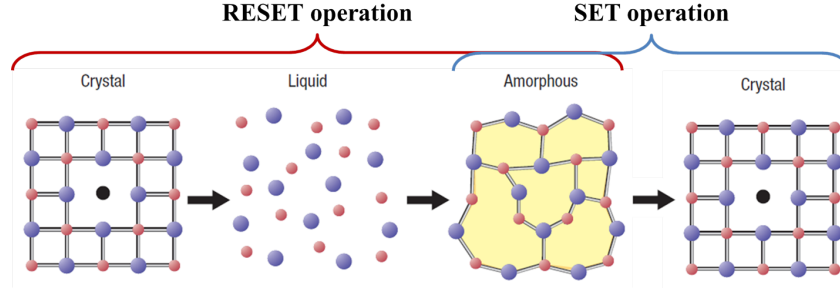


Figure 1.19: Principle of the phase change transitions. During the RESET operation, the material is melted then quenched to the amorphous phase. During the SET operation, the material is heated above T_c for a sufficient time to enable the reorganization of atoms into the crystalline phase. [Terao 2009]

fore simply achievable by the application of electrical pulses to the cell (fig.1.20): if the device is initially in a low resistive crystalline state, the amorphization of the chalcogenide (RESET or write operation) is achieved by raising the temperature of the material above the melting point T_m (650°C in GST) thanks to Joule effect, and then by quenching it in a disordered amorphous phase. The recovering of the crystalline state (SET or erase operation) is achieved by heating the phase-change material above the crystallization temperature T_c (150°C in GST) without exceeding the melting point. Both operations do not require the same amount of time nor energy: because of the high temperatures which need to be reached during the RESET operation, this step is the most power consuming. But it is also the shortest to achieve (typically a few tens of nanoseconds) when compared to the times needed during the SET operation to ensure the good recrystallization of the chalcogenide (usually in the 100 ns - 1 μ s range).

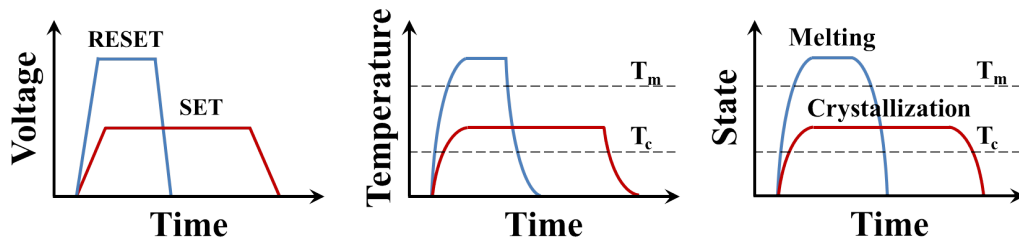


Figure 1.20: Schematic of the electrical pulses applied to program the cell into the RESET or SET state (left), along with the temperature profile inside the device during the pulses (middle) and the corresponding states of the phase-change material (right). [Hubert 2013]

1.4.3 I-V and R-I characteristics

A PCM device can be characterized by monitoring the evolution of the current passing through the cell as a function of the voltage (I-V characteristic), and the

evolution of its resistance as a function of the current (R-I characteristic).

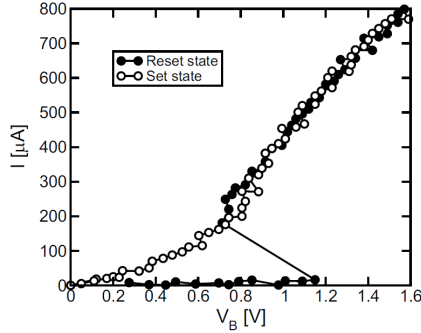


Figure 1.21: Typical I-V curve of a PCM device showing the SET & RESET characteristics, and the typical snap back observed for $V \geq V_{th}$ [Ielmini 2007a].

Fig.1.21 illustrates a typical I-V curve obtained on a 1R device. The SET state characteristic is splitted in two linear parts (ohmic conduction) while the RESET state characteristic is a bit more peculiar: when low voltage pulses are applied to the cell, the current stays very low because the phase-change material is in a very resistive amorphous phase. But when the voltage reaches a particular value V_{th} , the so-called threshold voltage, a switch is observed with a characteristic snap back in the I-V curve. This switching phenomenon is the heart of the PCM technology: once the threshold voltage is reached, the material switches to a high conductive state (ON-state) which allows the recrystallization of the chalcogenide thanks to the Joule heating induced by the increased current. The switching phenomenon thus enables the recrystallization of the material with only a few volts applied to the cell. Without this peculiar behavior, PCM devices would need much higher voltages to operate (tens or even hundreds of volts) and would be destroyed even before the beginning of recrystallization. While this phenomenon is essential for the functionality of PCM devices, its physical interpretation is still discussed [Wong 2010] and will be more detailed in section 1.7. The process described in this paragraph are summed up in fig.1.22.

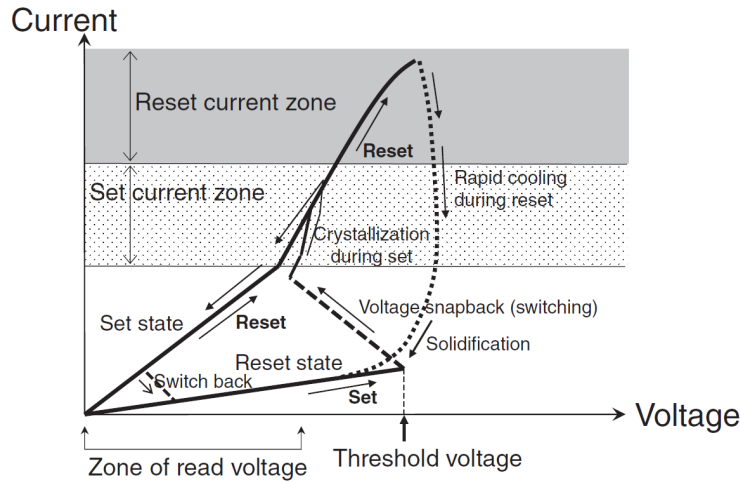


Figure 1.22: Schematic voltage-current characteristics of a PCM device [Terao 2009].

The resistance versus programming current characteristics of PCM devices allow to determine the amount of current needed to program the cells in the desired state. Fig.1.23 displays a classic R-I curve of a PCM device initially in a SET state or a RESET state. Each point corresponds to the final resistance of the cell achieved after the application of a current pulse of specific intensity. The graph is divided in three current ranges: the READ region at low currents corresponding to the values used for the reading of the devices; the SET region corresponding to the values needed to recrystallize the phase-change material, and the RESET region corresponding to the current values enabling the amorphization of the chalcogenide.

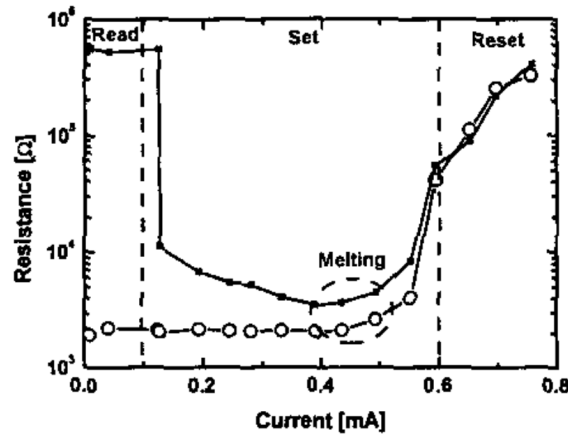


Figure 1.23: Classic R-I curves of a PCM device starting from a RESET state (filled circles) and from a SET state (white circles) [Pirovano 2003].

The physics of phase-change transformations will be discussed later in this chapter.

1.5 Strengths and weaknesses of Phase-Change Memories

1.5.1 Strengths

Write/erase speed The speed of the write (RESET) and erase (SET) operations is determined by the time needed to respectively melt and crystallize the phase-change material. As the melting of the material is a very fast process, the amorphization step, governed by the thermal constant of the cell, is a fast procedure which can be achieved in a few nanoseconds: studies have shown the feasibility of achieving a RESET state with 10 ns pulses [Ottogalli 2004]. On the other hand, the crystallization step is a longer process since more time is needed for atoms to be reorganized inside the material. The SET operation is typically achieved in times varying between a few tens of nanoseconds to a few microseconds, and is thus the limiting step of PCM operation speed. However, studies performed on $\text{Ge}_2\text{Sb}_2\text{Te}_2$ have demonstrated crystallization times shorter than 100 ns [ITRS 2012]. When

compared to Flash memories which typically need several tens of microseconds for the erasing operation, PCM cells are then much faster than NAND and NOR technologies.

Resistance window and endurance The resistance window of a PCM cell is defined as the gap between the resistances of the RESET and SET states. A good resistance window is thus necessary to distinguish both states. A typical $\text{Ge}_2\text{Sb}_2\text{Te}_2$ PCM cell exhibits resistance windows of at least 2 orders of magnitude, which is enough to ensure a good distinction between the two resistive states, and therefore a reliable reading of the information. The endurance of a memory device is defined as the number of write/erase cycles that one cell can sustain before failure. Concerning PCM cells, failures correspond to devices stuck in the low or high resistive state (because of interdiffusion of atoms inside the phase-change layer or voids creation for example), forbidding further programming. It has been demonstrated that the programming currents used to program the cells have a direct impact on their endurance: high programming currents will lead to faster failures [Lai 2003]. Endurance greater than 10^{12} cycles for a single device has been demonstrated, while typical values for Flash memories do not exceed 10^6 cycles.

Multi-Level capability The PCM technology also allows to store more than one bit per cell. These type of memories are called "Multi-Level Cells" (MLC) and represent an efficient way to increase the memory density, i.e. the number of bits per unit area. This technology can be achieved in PCM devices by different means:

- the first method consists in programming the PCM in an intermediate state between the SET and RESET states, either by partially amorphizing a cell originally programmed in a SET state, or by partially recrystallizing a cell originally programmed in a RESET state. This method has been proven to be functional with 2 bits per cell in a 256 Mbits demonstrator [Bedeschi 2009], and up to 4 bits per cell in smaller arrays [Nirschl 2007].
- the over way to store more than one bit per cell is to increase the number of active zones inside one cell, i.e. to use several layers of phase-change materials which can be amorphized or recrystallized instead of just one. For example it is possible to fabricate PCM cells with 3 phase-change layers in parallel [Oh 2009] or in series [Gyanathan 2012] to create 4 distinct resistive states and thus to store 2 bits per cell.

1.5.2 Weaknesses

Programming currents As it has been described previously, the writing operation is accomplished by melting and quenching the phase-change material inside the cell. It is thus necessary to heat the material above its melting temperature T_m , which is a very energy consuming step. High values of write current (called RESET current or I_{RESET}), typically $200 \mu\text{A}$ for 45 nm devices [Servalli 2009], are needed

to provide an efficient Joule heating, and this is one of the main PCM drawbacks since it directly affects the performances and the dimensions of the cells. Indeed, a full PCM device is made of the actual PCM cell in series with an access device (transistor or diode) which provides current to the cell: the more current is needed, the bigger the access device has to be. This is thus a limiting factor for scaling down the devices, and therefore a limiting factor to increase the density of the PCM technology. Moreover, since the memory arrays are powered by a limited source, a lower I_{RESET} would allow to program more cells in parallel, and increase the capacity of the arrays [Ahn 2005]. These are the reasons why the reduction of the RESET current has been one of the main topic of research since the beginning of PCM development. Several solutions can be considered:

- as the amount of current needed is directly proportional to the volume of phase-change material which has to be amorphized (the so-called active zone), decreasing this volume leads to smaller values of I_{RESET} . Since the active zone is defined by the contact area between the heater and the phase-change material as well as the thickness of the phase-change layer, efforts have been made to reduce those two parameters by exploiting new types of cell structures, which are described in section 1.6.
- the optimization of the cell structure can also enable a better confinement of current, leading to lower power consumption (see "confined structures" detailed in next section)
- another solution is to improve the interface between the heater and the phase-change material by adding a thin layer of a dielectric material. Indeed, studies have shown a large decrease of the reset current in PCM cells integrating a thin layer of TiO_2 or HfO_2 with up to 78% of current reduction compared to standard GST cells [Hubert 2011]. This reduction appears to be mainly due to a decrease of the equivalent contact area with the creation of small conductive filaments through the thin films, and a better thermal efficiency. In fact, the thermal conductivity of such materials being lower than materials used for the heater (typically tungsten or TiN), the thermal energy loss through the heater are lowered [Matsui 2006, Choi 2010], increasing therefore the temperature reached inside the phase-change material for the same amount of current. Less current is thus needed to program the cells integrating an interface layer.
- at last, it is also possible to modify the phase-change material itself by changing its stoichiometry or by doping it with elements like nitrogen, carbon or SiO_2 , which will modify the melting and crystallization temperatures of the material.

Programmed states stability Another challenge for the development of Phase-Change Memories is to limit the loss of data in the RESET and SET states, which results respectively from the recrystallization of the amorphous phase and the drift of the resistance. Indeed, the amorphous phase of chalcogenides is unstable: it tends

naturally towards recrystallization, which leads to the loss of data in the RESET state. This process is thermally activated, and while typical GST cells can remain in the RESET state for tens of years at room temperature, only a few papers show data retention longer than 10 years at 85°C (which is the typical criterion for non-volatile memories applications) for this material [Kim 2005, Pirovano 2004]. Data in the SET state can also be lost because of the drift of the resistance over time, which is a phenomenon well known for the RESET state but which can also be detrimental for the SET state. As these reliability issues are the main topic of this thesis, they will be described in more details in section 1.8 of this chapter.

1.6 Structures of PCM cells

As it has been introduced in section 1.5, the size of the cell, the volume of phase-change material to melt, the thermal and electrical confinements as well as the contact area between the heater and the phase-change material are key parameters when it comes to lowering the write current. Since the beginning of PCM history, many efforts have been made to find solutions enabling to minimize it by changing the structure of the cells. In the next sections, we present the evolution of PCM cells architectures as it can be found in literature.

1.6.1 Lance-type structure

Fig.1.24 describes the first PCM cell concept, known as the lance-type structure. This type of cell can be realized by the etching of a via in the dielectric material deposited over the bottom electrode. The via is then filled with a metal, typically tungsten or TiN, to create the plug. After this step, a chemical-mechanical polishing (CMP) is performed to ensure a good planarity of the surface, before the deposition of the phase-change material.

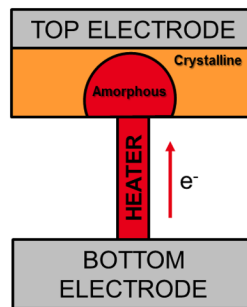


Figure 1.24: The lance-type structure.

The reduction of the contact area in the lance-type structure thus depends on the etching and lithography technology resolution available.

1.6.2 Edge structure

In an edge-type PCM cell, the heater is no longer vertical like in the lance-type structure, but horizontal. An example of this type of cell is proposed in fig.1.25. The phase-change material is deposited so that a lateral contact with the exposed surface of the heater is obtained.

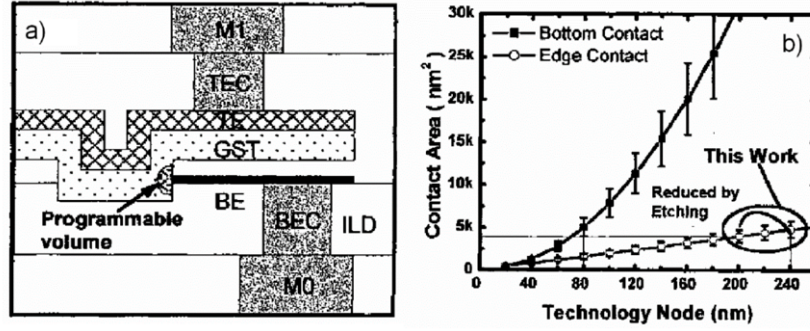


Figure 1.25: a) The edge-type structure. b) Comparison between the lance-type structure and the edge structure [Raoux 2008].

The contact area is thus defined by the thickness of the horizontal layer (BE) and its width. Results from [Raoux 2008] shows the advantages of such a geometry over the lance-type structure. However, difficulties are often encountered to ensure a perfect lateral contact with the material during the deposition.

1.6.3 Bridge structure

The bridge structure consists in two vertical electrodes separated by a thin insulating gap, and connected together only by a narrow line of phase-change material, hence the name "bridge structure". Fig.1.26 shows a schematic of this type of structure [Raoux 2008]. The gap between the two electrodes defines the bridge length (L). The phase-change material is deposited by magnetron sputtering to create the bridge, with thickness down to 3 nm (H), with a width (W) defined by electron-beam lithography, down to 20 nm [Chen 2008].

In this type of cell no heater is needed since the rise of the temperature is located inside the phase-change material (self-heating cell). Therefore, the cross-sectional area of the bridge ($W \times H$) defines the current needed for the RESET operation. The advantage of this structure is the possibility to achieve very small contact area dimensions, enabling to reach RESET current as low as 150 μA , but with an endurance not exceeding 30000 cycles [Chen 2006].

1.6.4 Confined structure

In a confined-type cell, the phase-change material is confined in the same hole than the heater, replacing it partially or totally (fig.1.27).

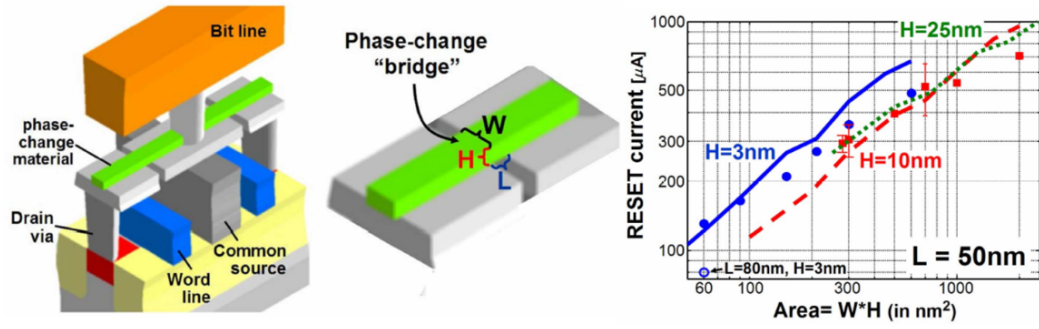


Figure 1.26: Scheme of the bridge structure (left) with the selector device, and experimental results for the RESET currents as a function of the cross-sectional area of the phase-change material, for different thickness H . [Raoux 2008, Chen 2008].

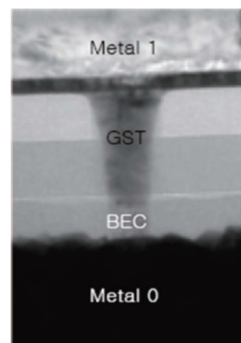


Figure 1.27: TEM images of a confined PCM cell [Lee 2007].

The confinement obtained by the surrounding dielectric material allows a better electrical confinement of the active volume, leading to lower I_{RESET} values. In addition to being very scalable, this structure shows indeed a big improvement on RESET currents, reducing more than twice the current needed for the write operation, and endurance up to 10^8 cycles [Lee 2007]. Just like standard lance-type cells, the contact area in confined cells is determined by the lithography resolution. The drawback of this architecture is that the whole volume of phase-change material is amorphized or recrystallized in the write/erase process. This is an issue when dealing with multi-bit capability since it is thus very difficult to achieve an intermediate state between the RESET state and the SET state.

1.6.5 μ trench structure

This type of structure was introduced in 2004 by STMicroelectronics [Pellizzer 2004] and is the structure used in the first real industrial PCM product. Fig.1.28 displays a schematic of a μ trench cell.

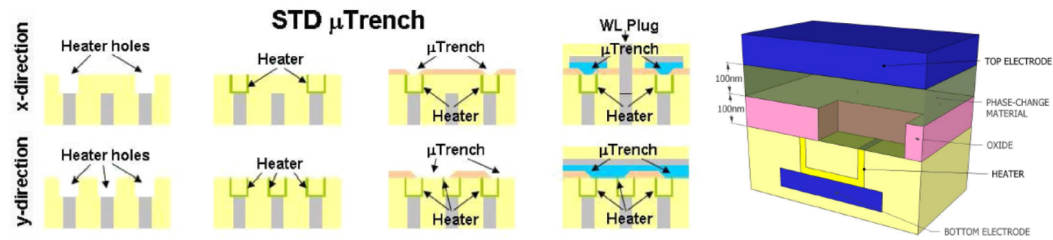


Figure 1.28: Schematic of a μ trench cell (right) and process flow (left, [Pirovano 2007]).

To fabricate a this type of structure, the bottom electrode and the dielectric material (SiO_2) are first deposited. Then a squared via is opened in the dielectric material by Deep UV (DUV) light lithography before the deposition of the metal layer (WSi in the case of the devices fabricated here at the LETI) to create the "ring". The via is then filled with the dielectric and a final CMP leaves the ring surface exposed. Another dielectric (SiN) is deposited and etch to open the trench, on which the phase-change material is deposited. The final step consists in the deposition of the top electrode. The contact area is defined by the control of the metal layer thickness, which therefore also defines the contact area and thus the RESET current.

1.6.6 Wall structure

Fig.1.29 shows a schematic of the wall-type cell. The wall structure is a direct evolution of the μ trench structure. It relies on the fabrication of a via in which a thin layer of a conductive material is deposited, etched, and then planarized, but unlike in the μ trench process, the PCM layer and the heater are etched at the same time (self aligned process). This structure is thus highly scalable, reaching sub-lithographic sizes. The result is a very small contact area between the heater and

the phase-change material, leading to lower RESET currents [Servalli 2009].

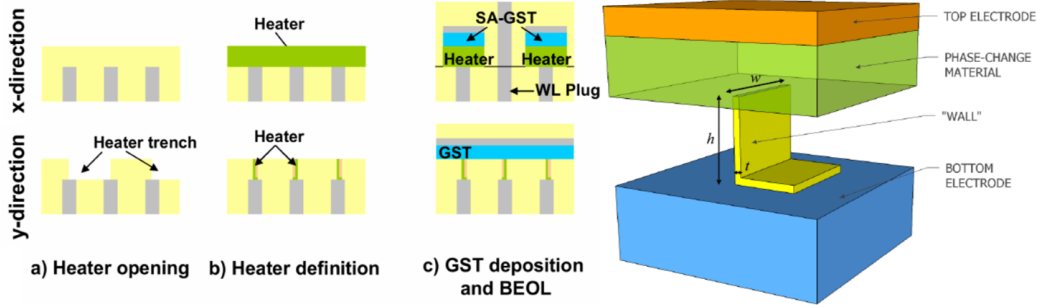


Figure 1.29: Schematic of a wall-type cell (right) and corresponding process flow (left, [Servalli 2009]).

1.7 Physics of crystallization in Phase-Change materials

The studies presented in this work have been performed in an effort to understand the physical process responsible for the loss of data in the RESET and SET states of Phase-Change Memories. As we have seen in section 1.5 when we introduced the drawbacks of Phase-Change Memories, the loss of data in the SET state comes from the resistance drift of the crystalline material, while the loss of data in the RESET state is due to the recrystallization of the amorphous phase. It is therefore important to understand the physics governing the crystallization of phase-change materials as it will enable us to identify the critical parameters involved, and give us the tools to develop a numerical model to simulate phase-change transitions. This numerical model, used for the simulations presented in chapter 4, is detailed in appendix B.

Two mechanisms are involved in the crystallization process of an amorphous material: nucleation, which initiates the crystallization by creating small crystalline nuclei, and then the growth of these nuclei enabling them to reach a macroscopic size.

1.7.1 Nucleation

The process implied during the nucleation step can be described by referring to the Classical Nucleation Theory (CNT). This theory developed by Gibbs in the 70's relies on the main assumption that the composition of the material stays unchanged during the crystallization and that the process is limited by diffusion.

Two types of nucleation can happen: homogeneous nucleation or heterogeneous nucleation. The homogeneous nucleation occurs at any site of the bulk material, while heterogeneous nucleation is ignited by the presence of preferential nucleation sites inside the amorphous material like impurities or interfaces.

Our numerical model used for the simulations takes into account both homogeneous nucleation, occurring in the bulk of the phase-change material, and heterogeneous nucleation, present around impurities and at the external boundaries of the

material. Only the heterogeneous nucleation is described in details hereafter, but homogeneous nucleation is treated in a similar manner.

As we have said, the heterogeneous nucleation model includes the presence of defects, impurities and other potential substrates like foreign particles which act as nucleation sites (fig.1.30) and add extra interfaces energies. The total free energy resulting from the creation of a square shaped nucleus in such a system is then given by equation 1.1:

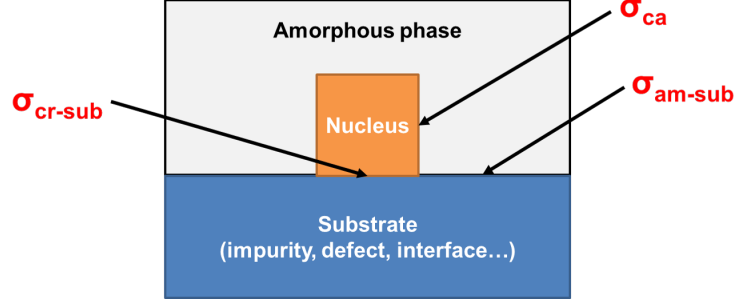


Figure 1.30: Schematic of the heterogeneous nucleation principle. Impurities, defects and other substrates contribute to the formation of nuclei by adding extra interfaces energies.

$$\Delta G = G_{am} - G_{cr} = r^3(-\Delta G_v) + 5r^2\sigma_{ac} + r^2\chi > 0 \quad (1.1)$$

Where r is the side length of the nucleus, σ_{ac} is the interfacial energy per unit area between the crystalline nucleus and the amorphous phase matrix, $\chi = \sigma_{cr-sub} - \sigma_{am-sub} < 0$ (in $J.m^2$) is the surface energy, describing the chemical affinity between the phase-change material and the surrounding materials (with σ_{cr-sub} and σ_{am-sub} being respectively the energies of the crystal-substrate and amorphous-substrate interfaces), and ΔG_v is the difference between the Gibbs free energy per unit volume of the amorphous and crystalline phase. ΔG_v represent the driving force of crystallization and is given by the relation Thompson-Spaepen (eq.1.2):

$$\Delta G_v(T) = G_{am} - G_{cr} = \frac{L_m}{T_m} \times T \times \ln\left(\frac{T_m}{T}\right) \quad (1.2)$$

Where L_m is the latent heat of melting and T_m the melting temperature of the material.

Knowing the values of the parameters L_m , T_m , ΔG_v , σ_{ac} and χ for the material of interest, we can plot the variation of ΔG as a function of the nucleus size r (fig.1.31).

The curve obtained shows a maximum at $r = r^*$. Given that $\frac{d\Delta G}{dr}(r^*) = 0$, we can calculate r^* :

$$r^* = 4 \frac{\sigma_{ca}}{\Delta G_v} \quad (1.3)$$

This parameter, of the order of a few nanometers, tends to infinity when T gets closer to T_m .

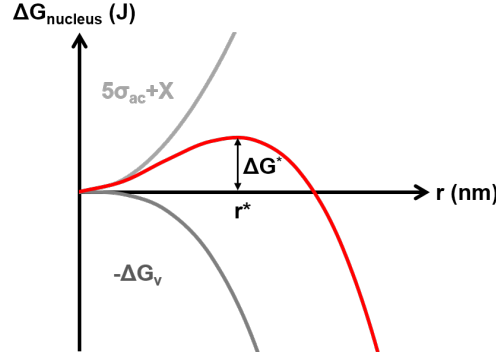


Figure 1.31: Variation of ΔG as a function of the nucleus size r for a given temperature. The curve shows a maximum at $r = r^*$ corresponding to the energy barrier ΔG^* which has to be overcome to create a stable nucleus.

The minimum energy needed to form a stable nucleus is thus given by:

$$\Delta G^* = \frac{4(\chi + 5\sigma_{ca})^3}{27\Delta G_v^2} \quad (1.4)$$

From here we can determine the rate of nucleation in stationary state, given by eq.1.5:

$$I_s = N \times \gamma \times O_n \times Z_e \times \exp\left(-\frac{\Delta G^*}{k_B T}\right) \quad (1.5)$$

Where N is the density of nucleation sites, γ is the atomic jump frequency, Z_e is the Zeldovich factor, and O_n^* is the number of atoms at the surface of the critical size nucleus which is given by, in the case of heterogeneous nucleation:

$$(O_n^*) = 5\left(\frac{r^*}{d}\right)^2 \quad (1.6)$$

Which leads to:

$$(O_n^*) \times (Z_e) = 0.456 \left(\frac{M}{\rho}\right)^{1/3} \sqrt{\frac{\chi + 5\sigma_{ca}}{RT}} N_a^{1/6} \quad (1.7)$$

With R the gas constant and N_a the Avogadro number.

The Zeldovich factor is given by equation 1.8:

$$Z_e = \left(\frac{\Delta G_{mol}(T)}{6\pi RT n^*(T)}\right)^{1/2} \quad (1.8)$$

Where $n^*(T)$ is the number of atoms inside the critical size nucleus and $\Delta G_{mol}(T)$ the molar free energy of the amorphous/crystalline transition (in $J.mol^{-1}$).

In the case of Phase-Change Memories, the electrical pulses applied to the cells imply a very fast increase and decrease of temperature (respectively in the order of 10^{12} K/s and 10^{10}). Because of this, a transient nucleation nucleation rate is used [Hyot 2002]:

$$I = I_s \exp\left(\frac{-\tau}{\delta t}\right) \quad (1.9)$$

in which τ is the time needed to establish the stationary state of nucleation and δt is the isothermal holding time based on the local temperature variation rate $\delta T/\delta t$. Knowing the values, for a specific material, of the thermodynamical parameters involved in this model, it is then possible to calculate the nucleation rate for any temperature. Fig.1.32 displays the nucleation rate in GST as a function of temperature (values for the thermodynamic parameters taken from [Gliere 2011]).

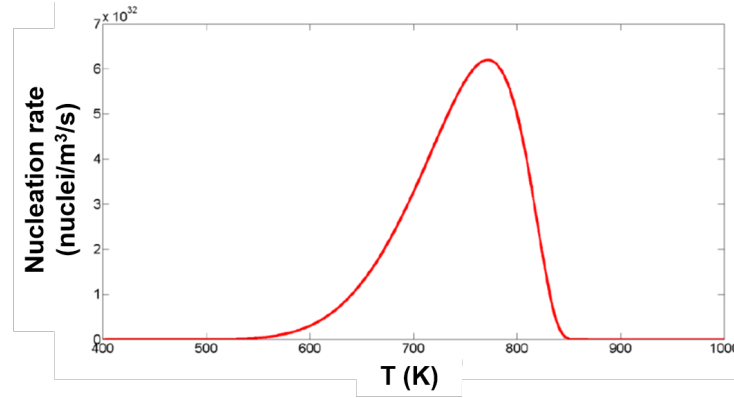


Figure 1.32: Evolution of the nucleation rate of GST as a function of temperature, showing a maximum around 800 K.

The gaussian-like shape of this curve, with a maximum around $T = 800$ K, is due to the fact that the nucleation mechanism is governed by two main forces: the driving energy of the crystallization (ΔG_v) and the atoms mobility, as shown in fig.1.33. At low temperatures (close to the glass transition temperature), the atomic mobility is low and so is the nucleation rate, even if the driving force of nucleation is strong. At high temperatures (close to the melting temperature), the atomic mobility increases strongly. However, the nucleation rate is still low because the driving force for crystallization is vanishing.

The nucleation rate rises and reaches its maximum at an intermediate temperature. This results from a trade-off between the two opposite effects which govern the mechanism.

1.7.2 Growth

Once the critical size is reached, the crystalline nucleus can start its growth phase. The growth of the crystalline grain is determined by the accretion of new atoms to the interface between the nucleus and its environment. This accretion depends on the probability that an atom goes from the amorphous phase to the crystalline phase, opposed to the probability that this atom goes back to the amorphous phase. The growth speed of a crystalline nucleus (in $m.s^{-1}$) is then given by:

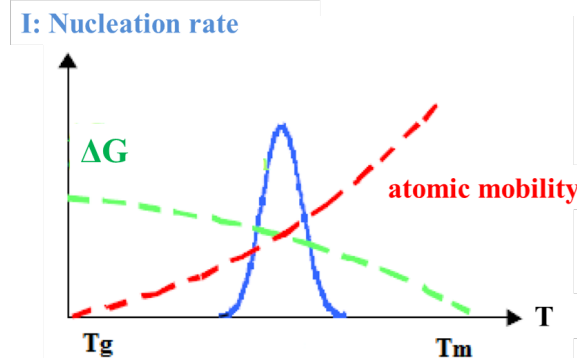


Figure 1.33: Schematic of the evolution of the nucleation rate of GST as a function of temperature.

$$v(T) = d \times \nu \times \left(\exp\left(-\frac{Q}{kT}\right) - \exp\left(-\frac{Q + \Delta G_v d^3}{kT}\right) \right) \quad (1.10)$$

In which ν is the atomic vibration frequency (in s^{-1}), Q is the energy barrier of the liquid to crystal transition (in J), and d is the interatomic distance. The term $\exp(-\frac{Q}{kT})$ represents the probability of an atom to overcome this energy barrier, while the other term $\exp(-\frac{Q + \Delta G_v d^3}{kT})$ represents the probability to go back to the liquid phase. If we remark that the accretion frequency of atoms on a crystalline nucleus can be written as follow:

$$\gamma = \nu \times \exp\left(-\frac{Q}{kT}\right) \quad (1.11)$$

We can write a new expression of equation 1.10:

$$v(T) = d \times \gamma(T) \times \left(1 - \exp\left(\frac{-\Delta G_v M}{9\rho RT}\right) \right) \quad (1.12)$$

With this new equation we can plot the evolution of the growth rate in GST, just as we did for the nucleation rate (fig.1.34).

Like the nucleation rate, the growth rate reaches its maximum between T_m and T_g . It is important to note that the highest growth rate is usually reached at higher temperatures than the maximum for the nucleation rate. These two mechanisms need to overcome a kinetic energy barrier, and nucleation needs to overcome a thermodynamic energy barrier due to the interface energy between the crystal and the liquid.

1.8 Reliability issues of Phase-Change Memories

In the case of a memory device, the reliability corresponds to the moment when it is not possible to write new data or to read them correctly. The reliability criteria for a PCM cell are the following ones:

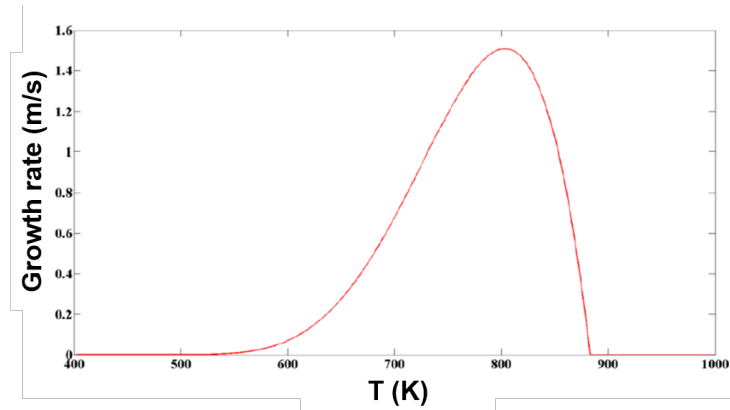


Figure 1.34: Evolution of the growth rate as a function of temperature in GST.

- Stability of data during the readings
- Endurance = number of write/erase cycles that the cell can achieve before failure
- Retention = Stability of data over time after programming for a given temperature

This last criteria contains two instabilities which are critical for the PCM technology:

- the spontaneous recrystallization of the amorphous phase after a certain amount of time, decreasing the resistance of the RESET state
- the structural relaxation of the material which is responsible for the increase of resistance over time (the so-called "drift" phenomenon), detrimental for the SET state.

In order to improve PCM cells performances, it is necessary to understand the process involved in the degradation of their reliability performances. In this section we will focus on the two instability issues exposed above.

1.8.1 Target specifications

To answer the needs of embedded applications, the cells must be able to sustain a temperature of at least 85°C for 10 years, and up to 150°C for automotive applications. However, these requirements are more restrictive for other embedded applications like Secure Smart-Card. For these types of application, the information must be precoded in the devices before the soldering of the chip on the electronic board for confidentiality & costs reasons. This soldering implies to expose the devices to temperatures up to 260°C for 2 minutes, which can lead to alteration of data. Indeed, the crystallization temperature of standard GST is 150°C, which means that

the cells precoded in the RESET states will recrystallize during the soldering step, and lose the information. It is thus necessary to optimize the phase-change material integrated in the PCM devices so that the cells can sustain such high temperatures without losing the data stored. This requirement (2min @ 260°C) will be the main target of the retention tests presented in the next chapter.

1.8.2 Retention of the RESET state

Failure mechanisms The amorphous phase of phase-change materials being thermodynamically unstable, it is subject to uncontrolled recrystallization after a certain time. The PCM cell initially programmed in a RESET state will progressively recrystallize, leading to a decrease of its resistance and thus a change of the cell state. This mechanism is thermally activated and time dependent.

In order to evaluate the RESET retention performances of a device, it is exposed to a given temperature and its resistance is followed over time. This way we can observe the evolution of the resistance as a function of time and detect the moment when the information is lost, thus giving the retention time of the cell for the specified temperature.

The mechanisms implied in the recrystallization of the amorphous phase are divided in three steps [Redaelli 2005]:

- Nucleation & growth inside the amorphous phase
- Formation of conductive filaments by percolation: the crystalline grains form a conductive path, leading to a decrease of the resistance
- Coalescence of crystalline grains and stabilization of the cell to a low resistance value

A theoretical model based on Monte-Carlo calculations has been developed by Lacaita [Lacaita 2007], which enables to follow the morphology of the phase and to calculate the crystalline fraction formed inside the amorphous region following the thermal annealing of the device at a given temperature (fig.1.35). The evolution of the cell resistance as a function of time is also determined.

From the retention curves measured at different temperatures, it is possible to evaluate the failing time for each temperature and obtain the Arrhenius plot displaying the crystallization time as a function of $1/k_B T$. By extrapolating these data we can determine the retention time of a cell for a given temperature, as depicted in fig.1.36.

The retention of the RESET state is a major topic of research in the PCM field, the objective being to find the best trade-off between a high crystallization temperature which fosters data retention, and short crystallization times for writing speed. To reach this goal, it is important to understand the physical mechanisms implied in the crystallization process and to identify the physical parameters which impact the retention.

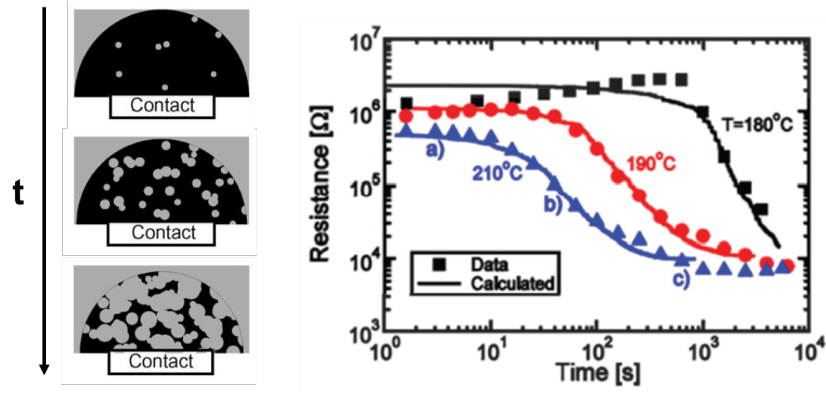


Figure 1.35: Simulation of the morphology evolution of a cell initially programmed in a RESET state (left, [Lacaita 2007]) and evolution of the resistance (measured and calculated) as a function of time for different temperatures (right, [Redaelli 2005]).

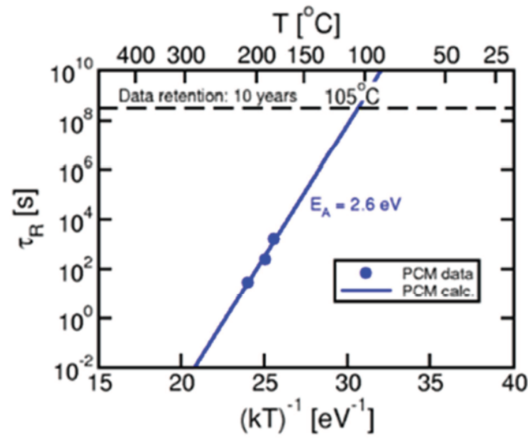


Figure 1.36: Arrhenius plot giving the retention time of a GeTe PCM cell as a function of the temperature.

1.8.3 Retention of the SET state

As it has been introduced in the section 1.5 of this chapter, the loss of data in the SET state results from the evolution of the cell resistance over time. Indeed, when following the resistance of a PCM cell over time, it appears that its value keeps rising, with a rate depending on the initial resistance of the cell [Ielmini 2007b]. This phenomenon called "drift" follows a power law as described in equation 1.13:

$$R = R_0 \times \left(\frac{t}{t_0}\right)^\nu \quad (1.13)$$

Where R_0 is the initial resistance measured at t_0 and ν is the drift coefficient.

Fig.1.37 shows a typical evolution of a device programmed in a RESET state or in a SET state. It appears that the drift is stronger in the RESET state, i.e. for high resistance values.

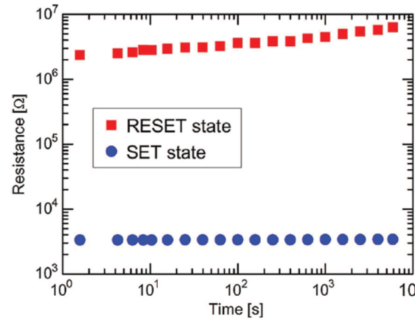


Figure 1.37: Evidence of the drift of the resistance over time, stronger for the RESET state than for the SET state [Boniardi 2010].

The resistance drift of the RESET state is a phenomenon already well known, attributed to the structural relaxation of the amorphous phase which tends to minimize its free energy, but the physics implied in this process is still debated. Several models have been proposed [Kim 2011]:

- reduction of the conductivity due to the trap decay, in the trap-assisted conduction model
- repositioning of the Fermi level by generation of the donor/acceptor defect pairs
- widening of the energy gap between the Fermi level and the mobility edge, caused by mechanical stress release.

However, all the models proposed in the literature take to the same power law empirical dependency of the resistivity on time leading to eq.1.13.

Because the resistance drift of the SET state is very weak in typical phase-change materials like GeTe or GST, it was considered to be negligible until recently. But in order to optimize the performances of PCM cells, new alloys have been introduced,

like germanium-enriched GST alloys, which enhance the thermal stability of the devices but also increase the drift of resistance over time for both RESET and SET states [Navarro 2013]. This increase, if too important, could take the cell to a resistance value higher than the threshold fixed for SET states, and is therefore detrimental for the good functionality of the device.

1.9 PhD goals & outline

In this chapter we have seen that the PCM technology is an already mature technology and one of the most promising alternative to current non-volatile memories like Flash, in a market which keeps growing every year. We detailed its working principle based on the reversible crystallization/amorphization of chalcogenide materials, and the typical PCM cell structures which enable to optimize the performances of the devices. We introduced the physics governing the crystallization process in phase-change materials, to finally come to the main topic of this work, namely the reliability issues of PCM devices.

The main goal of this thesis is to investigate on the physical origins of these reliability issues, in germanium-enriched GST devices. Lately, Ge-rich alloys have drawn a lot of attention thanks to their better thermal stability when compared to standard GST, leading to a better retention of the RESET state. But these alloys also have an impact on the resistance drift of the cell, which is increased for both RESET and SET states, eventually leading to the loss of data in the SET state as it will be detailed in the next chapter. If we want to limit this drift, it is of primary importance to understand its physical mechanisms, for both the RESET and SET states. This investigation is one of the main goals of this thesis, together with the understanding of how germanium enrichment improves the retention of the RESET state. To do so, we will first present the material and electrical characterizations performed on Ge-rich GST alloys and devices in order to evaluate their performances, with focus on the retention and drift results. The data obtained in this chapter will then be linked to the Transmission Electron Microscopy (TEM) analyses presented in chapter 3, where we take a closer look to the inside of the PCM cells. The structural and composition analyses, together with the results of simulations, will give us precious information about the mechanisms governing the phenomena in which we are interested.

Electrical characterization of Ge-rich PCM devices

In the previous chapter we described the PCM technology, its advantages, but also its drawbacks, and in particular the reliability issues which restrain the full development of PCMs. This chapter is dedicated to the study of devices integrating germanium-enriched GST alloys, showing why these materials have drawn so much interest lately. We will start the following section with the characterization of the materials used in our PCM cells, introducing the benefits of Ge-rich GST alloys over standard GST. We will then analyze the electrical performances of devices integrating those materials, with a statistical study of the SET & RESET characteristics, programming window, endurance and crystallization speed. In the last section we will focus on the analysis of the resistance drift of the SET state of our Ge-rich devices, as well as the retention performances of the RESET state.

2.1 Material characterization

In order to study the impact of germanium enrichment on the physical properties of the materials integrated in our cells, blanket layers of different Ge-rich GST alloys have been characterized, with germanium enrichment ranging from 25 at. % up to 45 at. %. During those experiments, the impact of nitrogen doping on these materials was also investigated, with concentrations up to 8 at.%. The reader should note that throughout the next sections, the composition in the label "GST + Ge %" refers to the percentage of excess germanium introduced in the reference alloy $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (as the deposition of the PCM layer is achieved by co-sputtering of a GST target and a germanium target).

2.1.1 Crystallization temperatures

As we have seen in the previous chapter, the crystallization of a phase-change material results in a decrease of its resistivity. By measuring the resistivity of the alloys as a function of temperature we can thus determine the crystallization temperature of the material under test. This type of characterization is performed by means of the 4-point probe measurement technique (fig.2.1) while heating up the wafers up to 400°C on a hot chuck, which allows to control the temperature ramp (up or down) from 1°C/min to 30°C/min. An example of a typical resistivity measurements as a function of temperature performed on a 100 nm $\text{Ge}_2\text{Sb}_2\text{Te}_5$ blanket layer and with

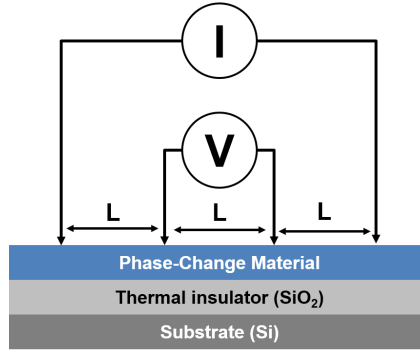


Figure 2.1: The 4-point probe measurement technique used for the resistivity measurements as a function of temperature of full sheets. All the probes are separated by the same length (≈ 1 cm). Current is applied by the two outer probes while the two middle probes measure the corresponding voltage. The resistance is then calculated using $R = \frac{\pi}{\log(2)} \frac{V}{I}$.

a ramp of $10^\circ\text{C}/\text{min}$ is shown in fig.2.2. From this curve, the crystallization temperature is determined by calculating the maximum of the resistivity curve derivative. The as fabricated material is amorphous, hence the high resistivity measured at low temperatures, but a sudden decrease of resistivity can be seen around 140°C , evidencing the crystallization of the material. After this first transition the material is in a face-centered cubic (fcc) configuration exhibiting a resistivity on the order of $10^{-4} \Omega\cdot\text{m}$. A second transition occurs for $T \approx 350^\circ\text{C}$, corresponding to the reconfiguration of the atoms into a hexagonal close-packed (hcp) phase.

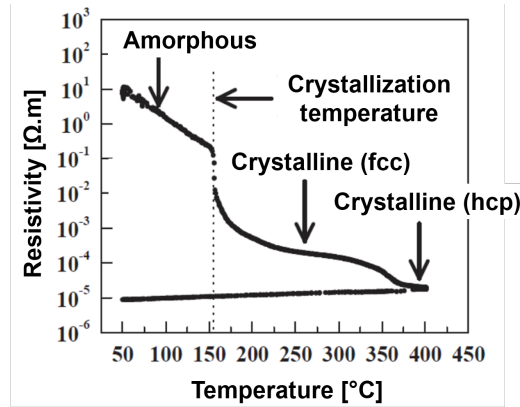


Figure 2.2: Resistivity measurements as a function of temperature performed on a full sheet of $\text{Ge}_2\text{Sb}_2\text{Te}_5$. A first transition is observed at $T=140^\circ\text{C}$ (amorphous to fcc), and a second one at $T=350^\circ\text{C}$ (fcc to hcp)

The results obtained on standard GST, GST + Ge35% and GST + Ge35% + N8% alloys are presented in fig.2.3. We can first notice the difference of the initial amorphous phase resistivities, as the GST + Ge35% and GST + Ge35% + N8% alloys exhibit higher values than standard GST. Then we can see that the decrease of resistivity start at higher temperature for the Ge-rich alloys, highlighting the benefits

of germanium enrichment on the thermal stability of the as-deposited amorphous phase, as the crystallization temperature rises from 140°C in pure GST up to 320°C in GST + Ge45%. The impact of nitrogen doping is more limited, as T_c saturates at 300°C for concentrations higher than 2 at.% in the GST + Ge35% alloy.

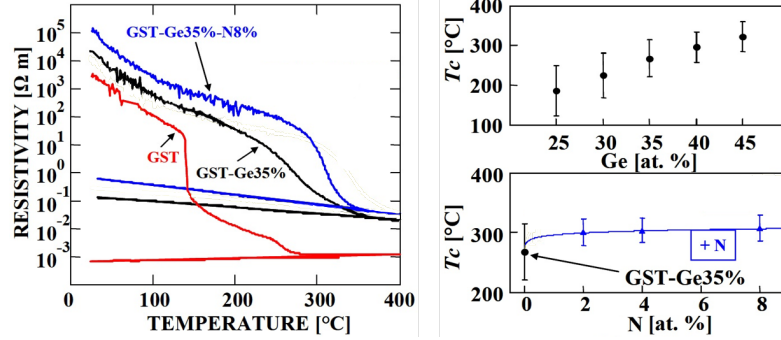


Figure 2.3: Resistivity vs Temperature for the materials under test, and the corresponding crystallization temperatures T_c , showing the increase of T_c with germanium enrichment and nitrogen doping.

After cooling down, the resistivity is still higher in the Ge-rich samples, meaning that the crystalline phase of these material is also more resistive than the crystalline phase of GST.

This improvement of the thermal stability of the amorphous phase is the main advantage of germanium enriched alloys over standard GST. This means that when integrated in a PCM cell, those materials will be more likely than GST to sustain high temperatures without recrystallization of the amorphous phase, and therefore to fulfill the "2 min @ 260°C" requirement of the soldering step.

2.1.2 Activation energies of conduction

During the resistivity measurements, all the samples have been annealed up to 400°C and cooled down to 25°C with a ramp rate of 10°C/min. From this ramp down we can extract the activation energy of conduction (E_C) of the crystalline phase for each material under test, calculated at room temperature according to the law $\rho = \rho_0 \exp(E_C/k_B T)$. The results are presented in fig.2.4 along with the final resistivity of the samples after cooling.

As it has already been observed in previous resistivity measurements, the resistivity of the crystalline phase is higher in Ge-rich sample than in pure GST, and increases with Ge content and nitrogen doping. The corresponding activation energy of conduction increases with germanium enrichment too, with 0.035 eV in the GST + Ge25% alloy up to 0.065 eV in the GST + Ge45% material. Nitrogen doping also causes the rise of E_C from 0.04 eV in the undoped GST + Ge35% alloy up to 0.075 eV in the 8% doped sample.

These data show that germanium enrichment and nitrogen doping tend to hinder the conduction inside the materials. More energy is thus needed to start conducting current in germanium rich GST alloys.

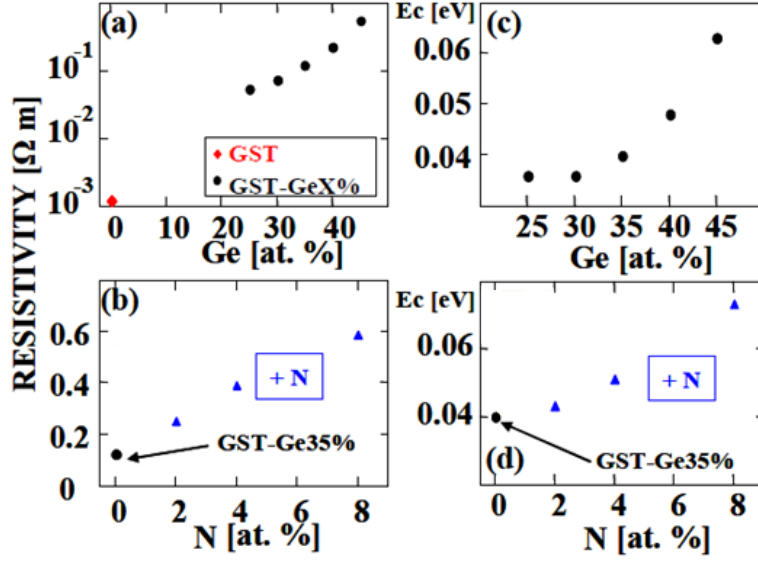


Figure 2.4: Resistivity of the crystalline phase of Ge-rich samples and activation energies of conduction.

We must note here that the activation energy of conduction as it has been calculated here is not representative of the conduction in the SET state of the final device, because our measurements have been performed on full sheets of phase-change materials with homogeneous composition, while the composition inside the devices can change, as it will be shown in chapter 4. However, These analyses are good way to study the impact of germanium content and dopants on the conduction of phase-change materials in an intermediate crystalline phase.

2.1.3 Kissinger analysis

To qualify the crystallization dynamics of a phase-change material, we can extract from the full sheet analysis the activation energy of this process (E_A) through the Kissinger analysis ([Al Ghamdi 2011, Kaban 2004]). This method is based on the fact that the measured crystallization temperature of a material depends on the temperature ramp which is applied to it, as shown in fig.2.5 [Friedrich 2000].

If we extract the crystallization temperatures for each ramp, we can determine the activation energy of crystallization by using the Kissinger equation (eq.2.1) [Kissinger 1957]:

$$\ln\left(\frac{v_T}{T_c^2}\right) = -\frac{E_A}{k_B T_C} + C \quad (2.1)$$

Where v_T is the temperature ramp, T_c is the corresponding crystallization temperature and C is a constant. Knowing the crystallization temperatures corresponding to each temperature ramp, we can plot $\ln\left(\frac{v_T}{T_c^2}\right)$ as a function of $\frac{1}{T_c}$. From here

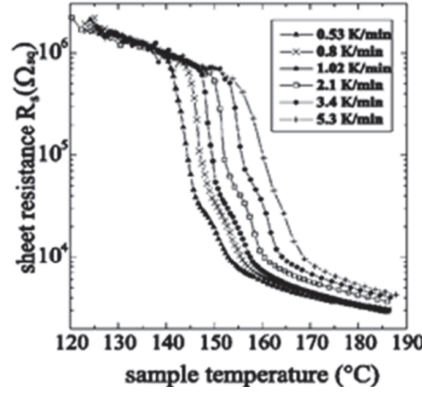


Figure 2.5: Evolution of GST resistivity as a function of temperature for different temperature ramps. The crystallization temperature is shifted towards higher values as the temperature ramp increases.

we can determine the slope of the curve fitting the experimental data, which is nothing else than E_A . Fig.2.6 displays the results of the Kissinger analysis for our Ge-rich alloys. The GST and GST + Ge45% alloys exhibit similar E_A values with respectively 2.8 and 2.7 eV, against 4.4 eV for the nitrogen doped alloy. These plots reveal that even if nitrogen doping doesn't have a strong impact on the crystallization temperature of the alloys, it is responsible for a strong boost of the activation energy of crystallization (more than 60%) with respect to the undoped sample. This means that nitrogen atoms inside the phase-change material hinder the crystallization process.

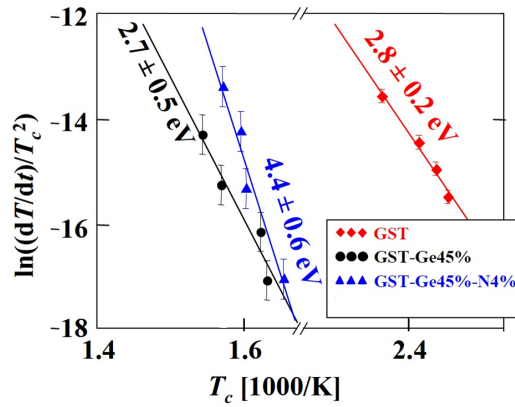


Figure 2.6: Kissinger plots of crystallization temperature obtained for the blanket layers under analysis, showing the boost of almost 60% of the activation energy of crystallization in the N-doped sample.

Besides, the very close values of E_A between the GST and GST + Ge45% alloys suggest that their crystallization dynamics are similar, and therefore that this process is dominated by the GST phase inside the Ge-enriched material.

2.1.4 X-Rays Diffraction measurements

XRD measurements were also performed to evidence the crystalline phases present in the germanium-enriched alloys after an annealing of 400°C, which corresponds to the highest temperature that PCM devices are exposed to, reached during the Back End Of Line step of the fabrication process. In the spectra displayed in fig.2.7 we can identify three peaks corresponding to the (111), (200) and (220) orientations of cubic GST, but also two peaks corresponding to the (111) and (220) orientations of cubic germanium.

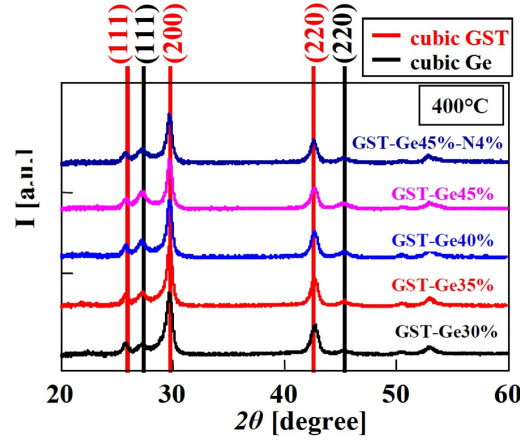


Figure 2.7: XRD performed on samples after 400°C annealing evidencing the segregation of cubic Ge.

The presence of these two peaks is the proof of the separation at high temperatures of Ge and GST phases in Ge-rich GST materials. This result will be very important when we will interpret the composition analyses of the devices presented in chapter 4.

Extracting the area of the peak corresponding to cubic germanium in the spectra of each alloy (fig.2.8), it appears that the fraction of cubic Ge is directly correlated to the total amount of germanium in the material. But the data also shows the strong effect of nitrogen doping on the formation of cubic Ge, as we can observe a significant reduction of the peak area in the 4% N-doped sample. This phenomenon could be explained by the formation of strong Ge-N bonds in the amorphous phase, keeping some of the germanium atoms to take part to the recrystallization process. [Caravati 2011].

The segregation of cubic Ge being an energetically expensive process, this explains the improvement of the thermal stability of the amorphous phase: the higher the content of germanium, the higher the energy needed for the system to initiate the phase separation between cubic GST and cubic germanium leading to the crystallization process.

The material characterizations presented above is a good starting point to understand the behavior of germanium-enriched GST alloys and their advantages over standard GST, especially concerning the thermal stability, which will be a key point

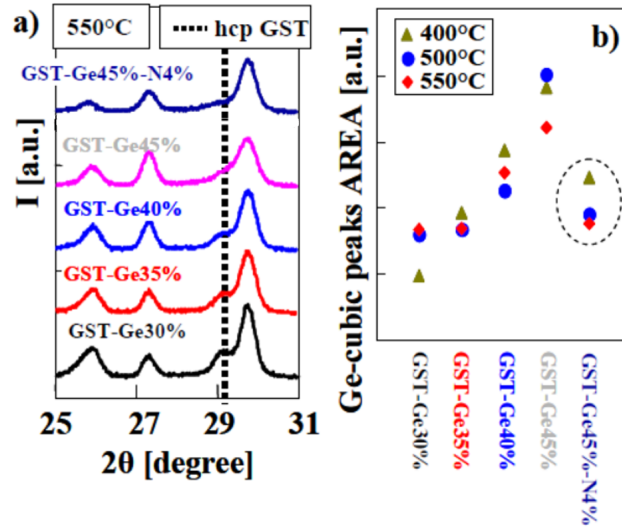


Figure 2.8: a) Evidence of hcp-GST phase at temperatures higher than 550°C. b) Area of cubic-Ge XRD peaks, indicative of phase concentration.

when dealing with the loss of data. We can now head on to the characterization of cells integrating those materials to determine their electrical performances test their data retention capabilities.

2.2 Electrical characterization of a PCM cell

2.2.1 Description of the PCM cells under study

In the first chapter, we saw that many different kinds of structures exist for the fabrication of PCM cells. The Ge-rich GST materials described in the previous section have been integrated in wall-type cells fabricated by ST Microelectronics, whose structure is presented in fig.2.9.

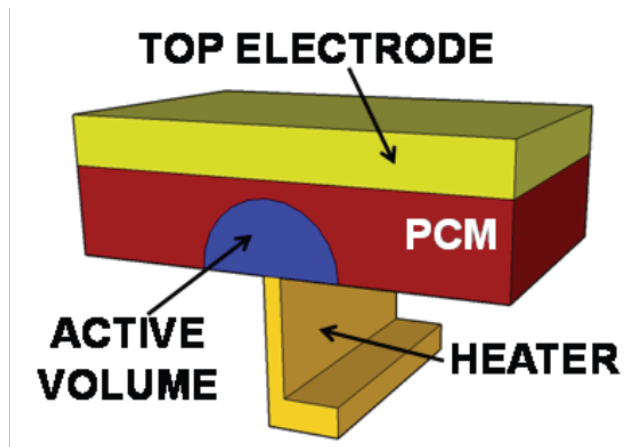


Figure 2.9: Schematic of the devices under test.

The active layer of Ge-rich GST material is deposited by co-sputtering of one GST and one germanium target using Physical Vapor Deposition (PVD) at room temperature (refer to appendix A for more details about the deposition technique). The as-deposited alloy is amorphous, but all the wafers undergo an annealing of 2 min at 400°C at the end of the fabrication process, which partially recrystallizes the material (as we have seen in the material characterizations section, some materials are not fully recrystallized at this temperature). Indeed, the industrial fabrication of PCMs implies an annealing of 400°C during the Back End Of Line (BEOL) steps: to recreate this step, all the wafers tested underwent an annealing of 400°C for 2 minutes at the end of the fabrication.

The heating of the phase-change material is done by the means of a resistive heater which provides a maximum temperature peak at the plug/phase-change material interface. Each electrode is linked to a metallic pad on the surface of the wafer which enables the application of electrical pulses. Depending on the characteristics of the electrical pulses (duration and amplitude), the devices can be programmed in a low resistive state (SET state) or in a highly resistive state (RESET state) by changing the crystallinity of the active volume (AV, referring to the volume where the phase-change transition occurs) respectively from crystalline to amorphous.

2.2.2 The equipment

Fig.2.10 represents a scheme of the experimental setup used for the electrical characterization of the devices. It includes a pulse generator (Agilent 8110A) which provides the electrical pulses applied to the cells, an oscilloscope (Tektronix TDS 744A) combined with two active probes (Tektronix P6205), a parametric analyzer (Keithley 4200-SCS) with current sensing resolution of 10 pA (which guarantees a high accuracy in the sensing of the cells), a Cascade Microtech probe station to automatically displace the wafers, and an electronic board.

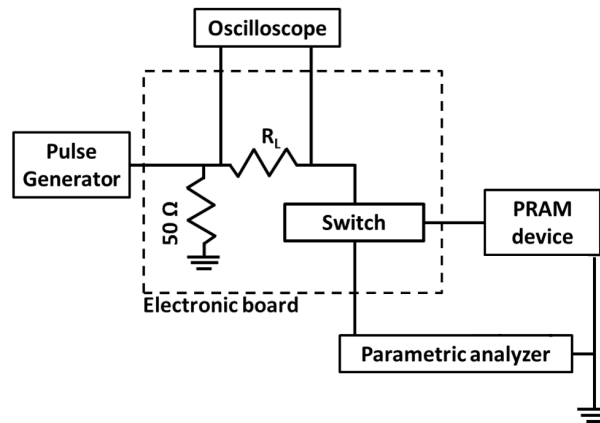


Figure 2.10: Experimental setup used for the electrical testing of the devices.

With this setup we can measure, thanks to the oscilloscope, the voltage of the electrical pulses provided by the pulse generator, and the voltage bias applied to

cell. The current flowing through the device during the application of the pulse is determined using the measurement of the voltage across the load resistance R_L of the electronic board which is linked to the oscilloscope: knowing the value of R_L , I is calculated following eq.2.2:

$$I = \frac{V_{Load}}{R_{Load}} \quad (2.2)$$

The load resistance has another important role as it also enables to limit the current during the switch of the cells, thus avoiding to damage them. The electronic board used in this setup (fig.2.11) was developed at the lab with the purpose to automatize all the electrical characterization process. It allows to remotely change the load resistance during the characterization, and the switch enables to link the PCM cell either to the pulse generator for programming, or to the parametric analyzer for the reading of the resistance after programming.

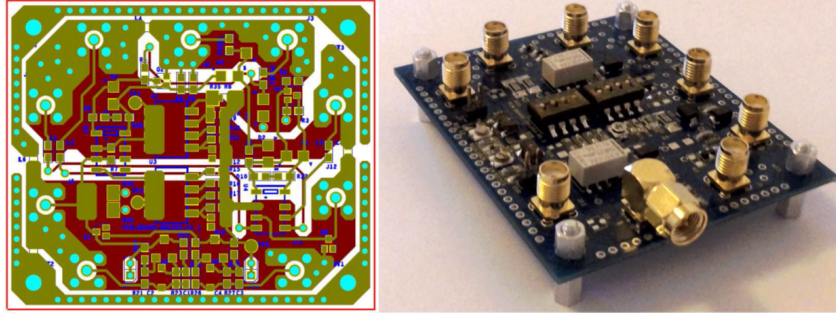


Figure 2.11: The electronic board used in the experimental setup described in fig.2.10.

The equipment is controlled *via* a software developed in Labview environment and enables all the standard characterization procedures (programming characteristics, low field measurements, data retention tests, cycling of the cells, etc.).

2.3 Devices performances

2.3.1 Seasoning

As said in the device description, all the wafers underwent an annealing of 2 min at 400°C at the end of the fabrication process. Because our Ge-rich materials are not fully recrystallized at this temperature, the devices are initially in an intermediate state which doesn't correspond to any of both RESET and SET states (see fig.2.12). To prepare the devices for the electrical characterization, a first "seasoning" step is thus applied to the cell. This step is made of 10 sequences of one staircase-up (SCU) followed by one staircase-down (SCD) both composed of a series of 50 pulses of increasing (SCU) or decreasing (SCD) voltage. Each pulse has a 5 ns rise time followed by a 300 ns plateau, and a 5 ns fall time.

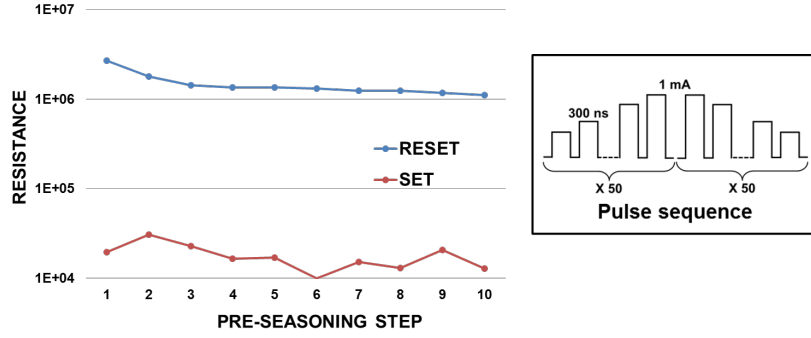


Figure 2.12: Example of a seasoning performed on one of the devices under test. The resistance of the RESET state is higher in the initial virgin state of the cell, decreases during the few first sequences before stabilizing itself around $1 \text{ M}\Omega$.

2.3.2 RESET characteristics

The RESET characteristics has been determined thanks to R-I measurements that we introduced in the first chapter. The results obtained on our Ge-rich devices are shown in fig.2.13. The devices are initially in a low resistive SET state because of the last step of the seasoning procedure (staircase-down). Starting from this state, a staircase-up sequence of 300 ns wide pulses (5 ns rise & fall time) is applied to each cell. After each pulse, the cell resistance is read in order to follow the amorphization process.

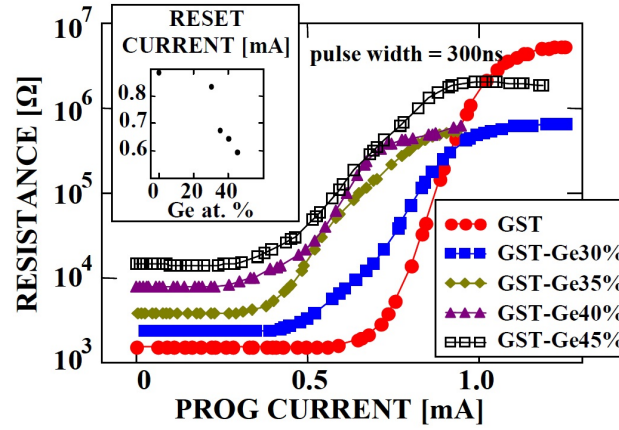


Figure 2.13: SET to RESET characteristics of the devices under test. The resistance of the SET state increases with Ge content. Ge-doping reduces the RESET current up to 33%.

First, as this was expected from the resistivity measurements presented in the material characterizations, the R-I curves show that the resistance of the SET states (i.e. crystalline phase) increases with germanium content, with a difference of one order of magnitude between pure GST and GST + Ge45%. Germanium enrichment also causes the decrease of the current needed to RESET the cell (taken as the current needed to reach 95% of the final plateau mean value), with up to 33%

reduction for the GST + Ge40% devices with respect to GST (repectively 0.6 and 0.9 mA).

The slopes of the curves also seem to be affected by Ge enrichment, as they become slighter with increasing Ge content. Several phenomena can explain this effect:

- First, as we have seen in the material characterizations, the germanium enrichment causes the presence of different crystalline phases in the material. Because of this, the number of boundaries inside the system rises, which increases the thermal conductivity of the material with respect to GST. The thermal efficiency of the device is thus improved, which leads to lower currents needed to start the amorphization.
- The second explanation involves the crystallization speed of the material (which will be detailed later in this section). If the material has a crystallization speed high enough (like GST), we can partially recrystallize the melted volume during the fall time of the programming pulse. In this case we can only start to increase the resistance of the device if the current of the pulse is high enough to leave a fully amorphized area close to the plug interface at the end of the pulse. Because of this, the higher is the recrystallization speed, the sharper will be the SET-RESET transition.

2.3.3 Endurance

The endurance of a PCM device is defined as the number of RESET-SET operations that a cell can sustain before failure. Even though endurance is one of the main advantages of PCM technology [Lai 2001], the thermal stress generated during the programming procedure, and especially during the RESET pulses where the phase-change material reaches its melting temperature, can generate mechanical failures such as delamination [Padilla 2011], local changes of the material composition, interdiffusion of the elements [Shin 2011].

The endurance is determined by following the evolution of the programming window as we apply a high number of identical RESET-SET cycles: the failure of the device is declared when the programming window becomes too small to correctly separate the SET state from the RESET state, or when the device is stuck in one of the two states. The results for our Ge-rich GST cells are reported in fig.2.14.

Note that for this characterization we used devices with shrunk dimensions with respect to the devices presented previously. The results show a stability of the RESET/SET operations up to 10^8 cycles, which is on the order of values expected for industrial applications.

2.3.4 Crystallization speed

The study of the crystallization speed of our Ge-rich devices has been performed using a new characterization procedure which enables to analyze the impact of the

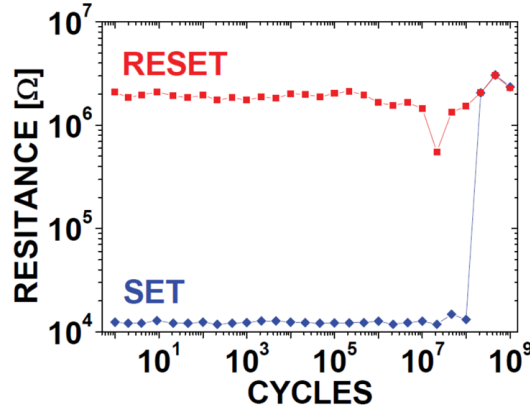


Figure 2.14: Endurance test performed on Ge-rich GST shrunk cells (RESET 30 ns, SET 800 ns) showing the stability of the RESET/SET operation up to 10^8 cycles.

main SET parameters on the crystallization speed. To do so, we start by programming a device in the RESET state, to which we apply a SET pulse with different current amplitudes and different time duration. The final resistance of the cell is read and stored after each RESET-SET sequence. This way, we can obtain a cartography of the SET resistance as a function of the pulse amplitude and time duration, which gives an idea of the electrical parameters allowing the achieving of a "good" SET state in the devices under test. Fig.2.15 shows the result of the characterizations performed on GST and Ge-rich devices. For these cartographies, we considered 2000 different SET current/time combinations, each point on the cartographies representing the mean value of the results obtained on 3 devices.

Thanks to these analyses we were able to investigate the impact of both pulse width and fall time of the SET pulse on the final resistance state of the devices. Concerning GST, the cartographies show that the SET state is easily obtained with a pulse of at least 0.4 mA of current amplitude and a width of about 150 ns or longer. The increase of the fall time (with a fixed width of 200 ns) allows to SET the cells even at high values of current. The cartographies done on the GST + Ge45% and GST + Ge45% + N4% devices show the reduction of the crystallization speed with respect to GST devices, but also the inefficiency of increasing the pulse width to achieve lower resistance states. Indeed, if the fall time is fixed at 5 ns for square-shaped pulses (minimum value), the devices are not able to reach resistances below $10^{5.5}\Omega$. In fact, these data indicate that increasing the fall time is a more efficient way to reduce the resistance of the devices, with a good SET state ($R \leq 10^{4.5}\Omega$) reached with a fall time of 300 ns or longer in the nitrogen doped devices. The particular "funnel-like" shape of the fall time cartographies hence shows that a low resistance state (LRS) can be achieved by tuning carefully the programming parameters.

These results were obtained using a one-pulse programming procedure. But here we also investigated the impact of procedures using a combination of several pulses to SET the cells. Fig.2.16 displays the R-I characteristics of devices integrating the

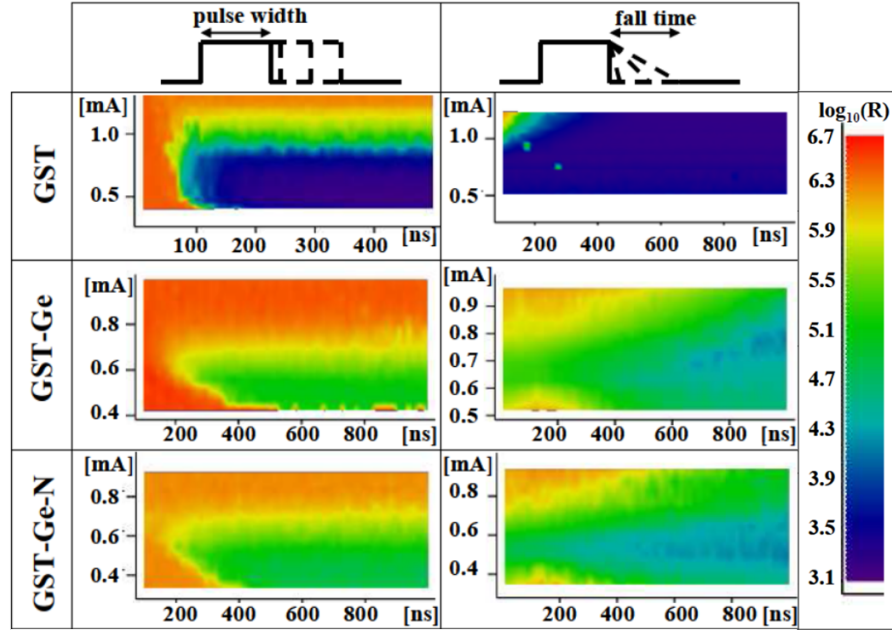


Figure 2.15: Cartographies of SET operation for all the materials under test. The increase of both width and fall time of the programming pulse applied to the cell (pre-programmed in the HRS) is investigated. Long pulse width is not sufficient to achieve complete recrystallization: only the control of the fall time enables the full SET.

GST+Ge45%+N4% material and programmed by means of two different stair-case down sequences (the first including 50 pulses and the second 10). The devices programmed with the 10 pulses sequence exhibit a higher final resistance than the ones programmed with the 50 pulses sequence. This demonstrates that the combination of specific pulse conditions can lead to optimized resistance states. In the case of the SCD procedures presented above, the 50 pulses SCD slowly decreases the current flowing through the cells until a value favorable for recrystallization, and then lower current amplitudes are gradually scanned with fine resolution, enabling the full recrystallization of the phase-change material. The 10 pulses SCD leads to the same favorable current level, but the following pulses are at lower current levels, yielding a SET resistance higher (i.e. worse crystallization), than the one obtained with the previous procedure.

2.3.5 The R-SET pulse

The R-SET pulse is an other multi-pulse procedure that we engineered in order to get a good current control in our 1R PCM cells. It consists in a combination of a RESET and a SET pulse, as described in fig.2.17.

This procedure allows to program the cells in a low resistance state with lower programming voltages than standard SET pulses. To do so, we take advantage of an interesting consequence of the structural relaxation (SR) of the amorphous phase described in chapter 2. Indeed, as soon as a cell is programmed in a RESET

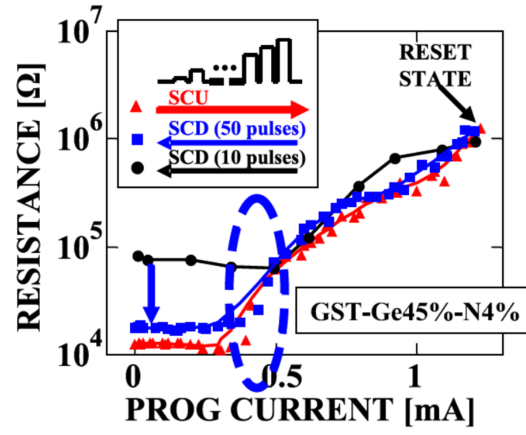


Figure 2.16: SET resistance as a function of the programming current, for two different SCD procedures (50 and 10 pulses). The 50 pulses SCD allows to reach lower values of resistance.

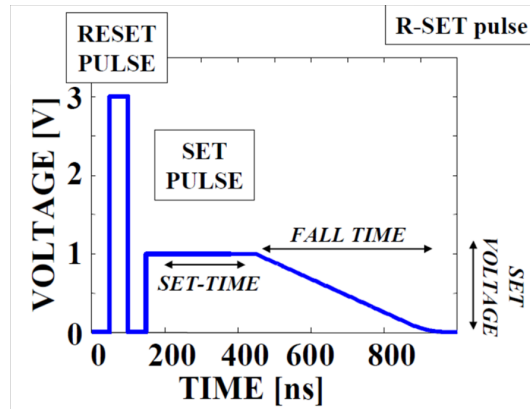


Figure 2.17: The R-SET pulse, a combination of a RESET and a SET pulse.

state, the SR of the amorphous phase induces the drift of both the resistance and the threshold voltage, which increase over time. Following the trap decay model described in ref. [Ielmini 2007a], the drift of the threshold voltage over time can be properly fitted with a power law, similarly to the resistance drift (eq.2.3):

$$V_{th} = V_{th,0} + \Delta V_{th} \left(\frac{t}{t_0} \right)^\nu \quad (2.3)$$

Because of this phenomenon, the threshold voltage of the cell is lower in the few nanoseconds following the RESET pulse. In the R-SET procedure that we used, the SET pulse is applied 5 nanoseconds after the RESET pulse, enabling to switch the cell with lower voltage values (and thus lower current) than if the SET pulse was applied seconds or minutes later. Fig.2.18 shows the consequence of the R-SET programming on the R-I characteristics of our cells.

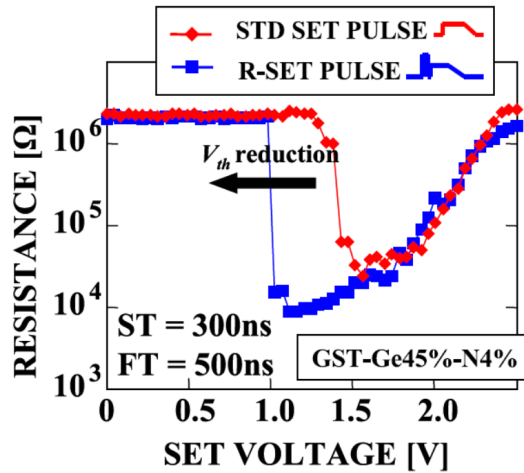


Figure 2.18: Comparison of programming characteristics of Ge-rich samples as a function of the programming procedure (standard SET or R-SET).

The standard SET procedure is not able to perfectly SET the cell, even with a careful tuning of the pulse width and fall time. In fact once reached the threshold voltage, the programming current is already too high with respect to the one needed for an optimized crystallization. On the contrary, with the R-SET procedure, the cell is switched at lower voltages, so we can reach a current value able to trigger the optimized crystallization process. With same width and fall time than the standard SET pulse, the R-SET procedure leads to a reduction of 33% of the voltage needed to SET the cell (1.5 V with the standard SET vs. 1 V for with the R-SET pulse).

Another consequence of the R-SET procedure is the reduction of the drift coefficient, which is studied in the next section.

2.4 Reliability study

2.4.1 Resistance drift of the SET state

In the first chapter, we showed that the drift phenomenon is strongly linked to the resistance of the device: the higher the resistance, the faster the drift. We investigated the impact of germanium enrichment on the drift of the cells by monitoring the evolution of their resistance over time. The drift coefficient is determined by fitting the experimental data with a power law function following equation 1.13 $R(t) = R_0(\frac{t}{t_0})^\nu$ introduced in the last chapter. In fig.2.19 we report the drift coefficients measured on GST + Ge45% devices as a function of their initial resistance.

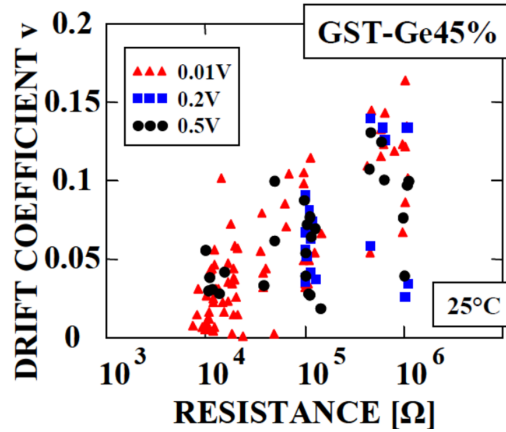


Figure 2.19: Drift coefficient measured at room temperature in GST + Ge45% devices showing the strong correlation of the drift with the initial resistance of the devices.

The measurements have been performed with three different read voltages, with no impact on the drifting behavior of the cells. This result, which seems to be in contradiction with what was published in [Padilla 2011], shows that the electric field doesn't affect the structural relaxations taking place in our Ge-rich cells.

The fact that we observe a strong reduction of the drift coefficient when we decrease the resistance of the cells leads us to correlate the drift of the SET state to the residual amorphous regions not involved in the recrystallization process [Ciocchini]. To minimize the drift of the SET state in the devices under test, we programmed the cells using a SCD sequence (which we will call the SETMIN procedure) comprising 50 pulses ($> 15\mu s$) to achieve the lowest SET resistance possible. The cells were then annealed at 150°C with log-time-spaced intermediate readings at room temperature (fig.2.20).

The results show the increase of the drift coefficient with increasing Ge content, while nitrogen doping act in the opposite way, as it softens the drift speed. This effect is not well understood, but it could be correlated with the decreased residual Ge amorphous phase, neutralized by the formation of stable Ge-N bonds as already shown in the material characterizations (fig.2.8).

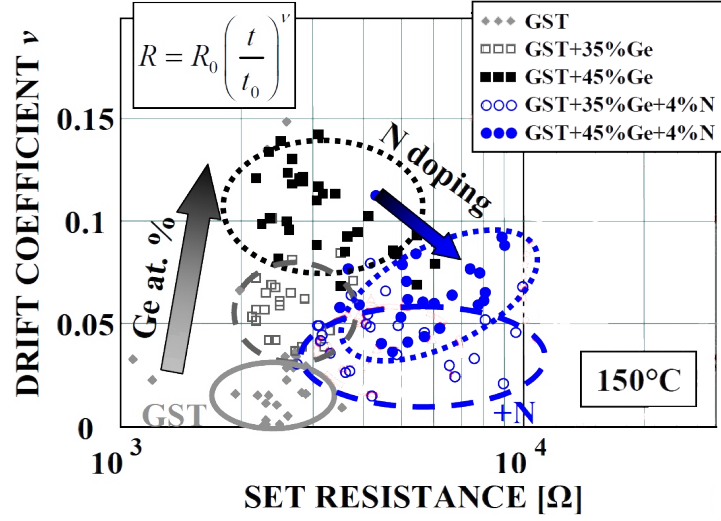


Figure 2.20: Drift coefficient calculated for the low resistive state of the devices under test.

We must note here that these results were obtained with a very time-consuming procedure, too long to address final applications. We thus compared the drift values for cells programmed with different procedures: the standard SET pulse, the SETMIN sequence and the R-SET pulse that we described in the previous section (fig.2.21).

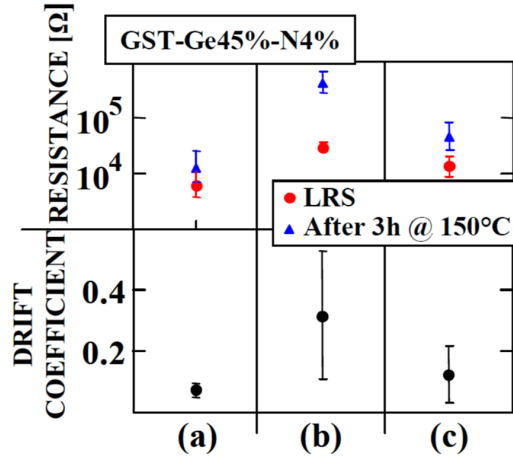


Figure 2.21: Comparison of the drift of the LRS obtained with three different programming techniques: a) Staircase-down ($> 15 \mu s$); b) standard SET (800 ns); c) R-SET pulse (800 ns).

The devices prepared with the standard SET pulse exhibit the highest initial resistance and drift coefficient, while the devices programmed with the SETMIN sequence show the smallest values of drift and initial resistance. The results highlight the benefits of the R-SET procedure with respect to the standard SET programming, with drift values approaching the ones obtained with the SETMIN sequence while maintaining a programming time compatible with industrial applications ($< 1 \mu s$).

2.4.2 Retention of the RESET state

As already stated in the first chapter, the amorphous phase formed in the RESET state is unstable and tends to recrystallize after a certain period of time, leading to the loss of the information stored.

We tested the data retention of the RESET state in our Ge-rich devices through the monitoring of the resistance of 20 devices over time during a constant annealing provided by the thermal chuck of the probe station. The criterion considered for the failure of the devices is the reaching of a resistance value equal to half the initial resistance. The results are then extrapolated assuming that the failure time (considered as the time necessary for the failure of 50% of the devices) has an Arrhenius dependency as exposed in equation 2.4:

$$t_{fail} = t_0 \exp\left(\frac{E_A}{k_B T}\right) \quad (2.4)$$

Where t_0 is a fitting parameter, E_A is the activation energy of the failure process and T is the temperature used for the accelerated retention test. Thanks to this equation we can extrapolate the maximum temperature to guarantee 10 years of retention for at least half the devices, as well as the maximum failure time expected at a given temperature. The results of these Arrhenius plots, displayed in fig.2.22, show the improvement of the data retention thanks to Ge-enrichment with retention times (10 years at 210°C for GST+Ge45% and 208°C for GST+Ge45%+N4%) among the best reported in literature [Czubatyj 2010].

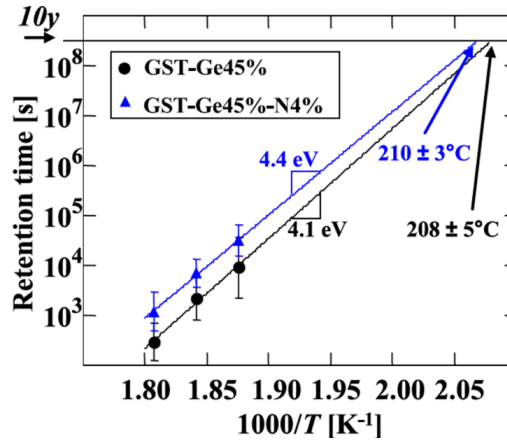


Figure 2.22: Arrhenius plot of data retention time for GST+Ge45%, with and without nitrogen doping, showing a retention time of 10 years at respectively 210 and 208°C among the best results reported in literature [Czubatyj 2010].

The retention of both the RESET and SET state was also evaluated using an Isochronal Annealing Steps Procedure (IASP) at successively higher temperatures (from 220°C up to 260°C): the devices under test are first programmed in the desired state and left at room temperature, with reading of the resistance after one hour to evaluate the resistance drift; they are then annealed for one hour at 220, 240 and

260°C with readings in between each annealing. Fig.2.23 shows the results of the IASP performed on our devices.

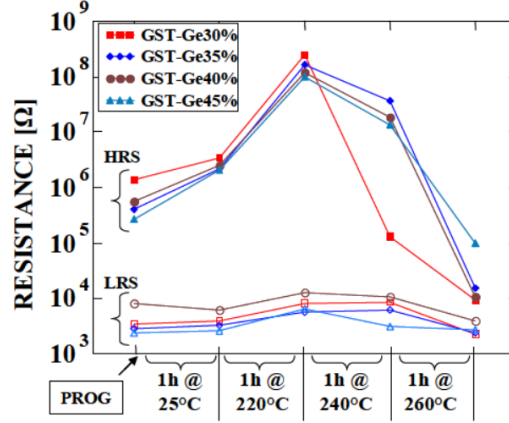


Figure 2.23: Isochronal Annealing Steps Procedure(IASP) at successively higher temperatures performed on Ge-rich GST devices. Drift of the HRS state is observed during the first two steps, followed by the recrystallization of the amorphous phase causing the decrease of resistance. Best stability is observed for the GST + Ge45% devices which are not fully recrystallized at the end of the procedure.

For all the devices under test, we observe an increase of the RESET (or HRS) resistance during the two first steps, and then its decrease, causing the closing of the programming window. This shape is due to the effect of two phenomena: first, structural relaxations of the amorphous phase causes the drift of the resistance towards higher values, while the decrease of the resistance results from the recrystallization of the material. These data show that Ge enrichment increases the stability of the RESET state, as the GST + Ge45% devices are not fully recrystallized at the end of the procedure.

2.5 Chapter conclusion

The results presented in this chapter provide us a full description of the electrical performances of our Ge-rich devices. The full sheet analyses performed on Ge-enriched GST alloys (with or without nitrogen doping) have shown the improvement of thermal stability with germanium content, as well as a strong boost of the activation energy of crystallization thanks to nitrogen doping. The XRD measurements evidenced the phase separation between GST and cubic germanium, thus explaining the improvement of thermal stability in Ge-rich alloys as the system needs more energy to initiate the phase separation leading to the crystallization process. The electrical characterization performed on wall-type devices integrating these Ge-rich alloys showed the reduction of RESET currents and the increase of the initial SET resistance with germanium enrichment, as well as suitable programming window and endurance for industrial applications. The crystallization speed study of the Ge-rich devices showed the importance of the fall time parameter when applying a single

electrical pulse to the cells to obtain a good SET state, but also that multi-pulse procedures like the stair-case down sequence could lead to lower resistance values. Another multi-pulse procedure, called the R-SET pulse, has been engineered, enabling to SET the cells with lower voltage values and comparable programming times than standard SET pulses. The drift of the cells have also been evaluated, showing the increase of drift coefficients with Ge content, but also the softening of the phenomenon with nitrogen doping. The procedures used to program the cells also has an impact on their drifting behavior: the staircase down sequence exhibits the lowest drift coefficients, but also the longest programming times ($> 15 \mu\text{s}$) while the R-SET pulse allows to reach smaller drift coefficients than the standard SET pulse, with suitable times for industrial applications. At last, the retention tests conducted on the RESET states of our Ge-rich devices showed results of 10 years retention at 210°C , which are among the best results reported in literature [Czubatyj 2010]. Thanks to the electrical characterizations performed on our Ge-rich devices, we can now choose the programming states which will be interesting to study through TEM analyses, in order to go deeper into the understanding of the reliability issues in which we are interested. This study is the object of the following chapter.

TEM analyses of Ge-rich PCMs & Simulation Studies

As explained in the previous chapter, the main reliability issues of PCM devices (namely the drift of the SET resistance and the retention of the RESET state) are strongly linked to physical phenomena taking place inside the device, in the phase-change material, at the nanoscale. In order to understand the origins of these phenomena, a detailed analysis of the evolution of the phase-change material (structure, composition...) is thus needed. Transmission Electron Microscopy (TEM) is the most efficient technique to answer those needs, as it enables not only to acquire high resolution images of the devices, but also to analyze their structure and their composition thanks to characterizations such as Dark Field (DF) imaging, Diffraction Patterns (DP), Energy Dispersion Spectroscopy (EDS) or Electron Energy Loss Spectroscopy (EELS). In this chapter, we first describe how we programmed the cells and prepared the samples for TEM analysis with the help of the Focused Ion Beam (FIB) tool. We then proceed to the presentation of the results obtained through the previous mentioned characterizations for some of the samples under test, keeping the last section for a discussion on the data which were gathered.

3.1 Sample Preparation

Here we detail the procedure which was systematically used to prepare the samples for TEM analyses. Regarding the electrical results presented in the last chapter, it appears that the devices integrating the GST + Ge45% + N4% offers the best trade-off between SET/RESET characteristics, resistance drift and retention capabilities: it was thus decided to concentrate our efforts on this material.

3.1.1 Electrical characteristics and programming of the devices under analysis

As said in the last chapter, the devices under test underwent a first seasoning step to ensure their stable behavior throughout cycling (except a few devices that we kept virgin for a specific programming state - see Multi-RESET hereafter). This seasoning also enables us to exclude the devices which are not functional (stuck in the RESET or SET state) and select the ones which will be prepared for TEM analyses. Among all the devices integrating the GST + Ge45% + N4% alloy, we picked out 20 of them, with electrical performances representative of the global characteristics presented in

chapter 3. The R-V characteristics of the selected devices are displayed in fig. 3.1. The cells were initially programmed in a high resistance state, so that we could observe the drop of the resistance resulting from crystallization when increasing the voltage, and thus determine the voltage to SET the cells.

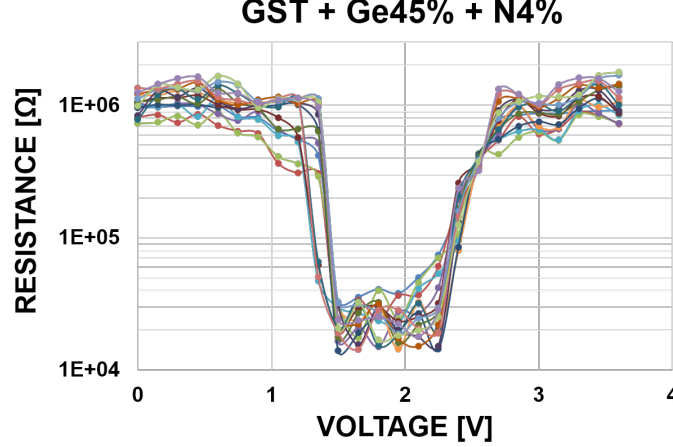


Figure 3.1: R(V) characteristics of the GST + Ge45% + N4% devices selected for further TEM analyses. The crystallization of the cells starts at $V \approx 1.5$ V. Full re-amorphization is obtained for $V \geq 2.8$ V.

The devices exhibit an initial RESET resistance comprised between ≈ 800 k Ω and ≈ 1.2 M Ω . The drop of the resistance, corresponding to the recrystallization of the amorphous phase inside the cells, starts at ≈ 1.3 V, and the SET state is reached in all the devices at ≈ 1.5 V with resistances ranging from ≈ 10 to ≈ 40 k Ω . The resistance then starts to increase again around 2.2 V because of re-amorphization, which is completed in all the devices at 3 V, showing a final RESET resistance of the order of 1 M Ω .

Now that we know the voltages needed to SET or RESET each device, we can control their resistance level and program them in the desired states. We defined 5 electrical states interesting for the following TEM analyses:

- the RESET state which is the high resistance state defined previously;
- the standard SET state, which corresponds to the low resistance state reached with a simple single pulse;
- the Multi-RESET state, a high resistance state programmed with a series of 10 millions of RESET pulses, applied to a virgin cell which wasn't seasoned;
- the SETMIN state, introduced in last chapter, programmed with a staircase down sequence;
- the R-SET state, also introduced in last chapter, programmed with a combination of a RESET and a SET pulse.

The RESET and SET states devices will be used as references during the TEM analyses for comparison with the cells programmed in the other states. The Multi-RESET devices were prepared to study the impact of the RESET pulses on the migrations of elements inside the phase-change material. Indeed, regarding the first TEM results obtained on early test samples, and according to other studies [Du 2015], the RESET operation induces atomic migrations during the melting of the material, which can lead to reliability issues. The purpose of the Multi-RESET sequence was then to emphasize these migrations inside our Ge-rich devices, to clearly see the tendencies and decorrelate the contributions of the RESET pulses from the SET pulses. The SETMIN state corresponds to the lowest resistive state achievable, which is reached by applying a staircase down of 50 pulses to the cell. At last, devices were programmed with two types of R-SET pulses: one with a trailing edge and one without one (R-SET A & R-SET B). The details of the electrical pulses used for each programming state are summed up in fig.3.2. The width and fall time of the standard SET and R-SET pulses were purposely increased with respect to the values used for the electrical characterizations of the last chapter, in order to emphasize the effect of the pulses on the structure of the cells.

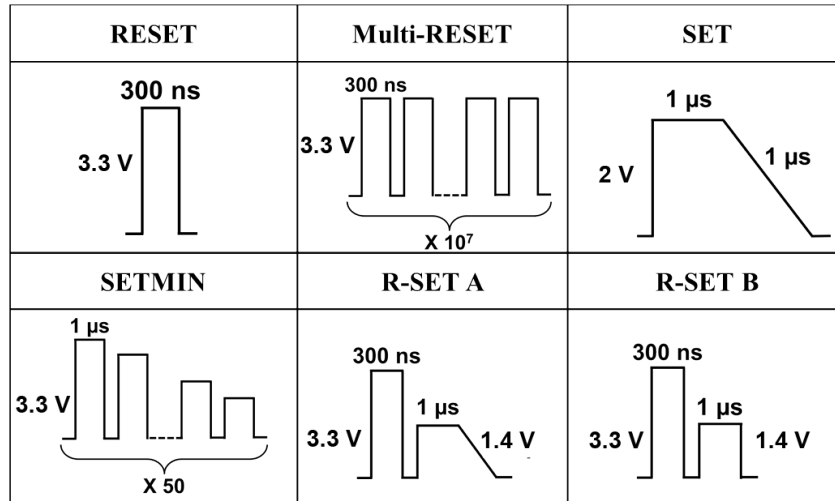


Figure 3.2: Details of the electrical pulses used for the programming of the devices under analysis.

After programming, the resistance of the devices has been monitored to determine the drift coefficient of each cell. The results of these measurements are reported in fig.3.3 together with the initial resistance of the devices under analysis. From the 20 initial devices, 7 of them were destroyed during FIB preparation (see below), so only the 13 remaining devices are presented here. They exhibit the same tendencies that the ones we presented in the last chapter: the RESET and Multi-RESET devices show the highest resistances (1.2 M Ω for RESET #1, 894 k Ω for RESET #2 and 4.5 M Ω for the Multi-RESET device) and drift coefficients (respectively 0.16, 0.15 and 0.17). The standard SET cells have resistances ranging from 28 to 46 k Ω , with drift coefficients of 0.122 and 0.136, while the SETMIN cells show the lowest

resistances with 3.1, 4.6 and 2.6 k Ω with also the smallest drift coefficients (respectively 0.051, 0.054 and 0.048). We can also observe the difference of resistance level and drift between the R-SET A and the R-SET B devices: the R-SET A cells have resistances comprised between the SETMIN and the standard SET values with 11 and 14 k Ω and drift coefficients of respectively 0.104 and 0.107, while the R-SET B cells show higher resistances, above the standard SET values, with 58 and 95 k Ω and drift coefficients of 0.135 and 0.142.

	Device Id	Resistance	Drift coeff.
RESET	RESET #1	1.2 M Ω	0.16
	RESET #2	894 k Ω	0.15
Multi-RESET	Multi-RESET	4.5 M Ω	0.17
Std SET	SET #1	31 k Ω	0.122
	SET #2	28 k Ω	0.122
	SET #3	46 k Ω	0.136
SETMIN	SETMIN #1	3.1 k Ω	0.051
	SETMIN #2	4.6 k Ω	0.054
	SETMIN #3	2.6 k Ω	0.048
R-SET A	R-SET A #1	11 k Ω	0.104
	R-SET A #2	14 k Ω	0.107
R-SET B	R-SET B #1	95 k Ω	0.142
	R-SET B #2	58 k Ω	0.135

Figure 3.3: Programming resistances and drift coefficients of the devices under analysis.

This difference of resistances and drift coefficients between the R-SET A and R-SET B devices suggests that a better recrystallization is obtained when increasing the fall time of the SET pulse in the R-SET procedure, which is in accordance with the results presented in the last chapter when we studied the crystallization speed of our devices.

The devices are now ready to be prepared for TEM analyses, which will give us more information about the morphological differences between the cells.

3.1.2 Extracting the devices

This step is the most critical step in the preparation of the samples for TEM observations, because it implies the use of a Focused Ion Beam (FIB) to mill the wafer in the vicinity of the device. A description of this equipment and his working principle are given in appendix.

The FIB preparation is a destructive technique which rises several challenges:

- because of the small dimensions of the devices, great care must be taken in their localization. This is the most delicate part, because an error of a few tens of nanometers can result in the destruction of the device;
- the energy of the ion beam, comprised between 2 and 30 keV, causes the rise of the temperature inside the phase-change material, which can lead to the alteration of its structure, especially in the RESET devices if the crystallization temperature is reached. To avoid this effect, the energy of the beam is reduced when approaching the location of the cell, thus keeping the phase-change material from recrystallizing;
- the Secondary Electrons Microscopy (SEM) imaging which is used during the FIB preparation to check the advancement of the milling induces the use of an electron beam, which can also alter the samples. The electrons sent on the sample must indeed find a way out; if not, they will cause ElectroStatic Discharges (ESDs) which can eventually destroy the cells, as we will show in this section.

Fig.3.4 shows a 3D schematic of the devices which were prepared. Before the first milling, a $2\ \mu\text{m}$ thick layer of tungsten is deposited by ion beam gas-assisted deposition (see appendix B) on the sample surface, above the device position (fig.3.5). The role of this sacrificial layer is to protect the cell during the milling, which causes the ablation of a part of the sample surface.

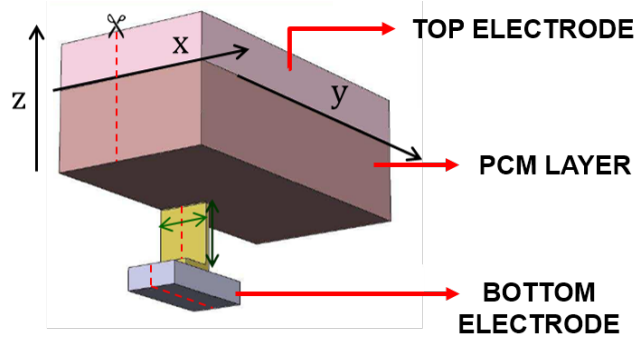


Figure 3.4: 3D schematic of the devices under FIB preparation.

After the deposition, a first cut is made perpendicular to the Y axis. This enables us to locate the lines (top and bottom electrodes) which are connected to

the device, and thus to determine its position. Once this is done, the sample is rotated and two other cuts are made perpendicular to the X direction, isolating a small piece of wafer, the so-called "chunk", which contains the device. The sample is now ready to be extracted from the wafer, thanks to a tungsten needle (Omniprobe, see appendix B). The needle is used as a fishing rod to take out the sample and fix it to a copper grid dedicated to TEM analyses. The soldering of the sample on the Cu grid is accomplished using ion beam assisted tungsten deposition with the gas injector system of the FIB (fig.3.6).

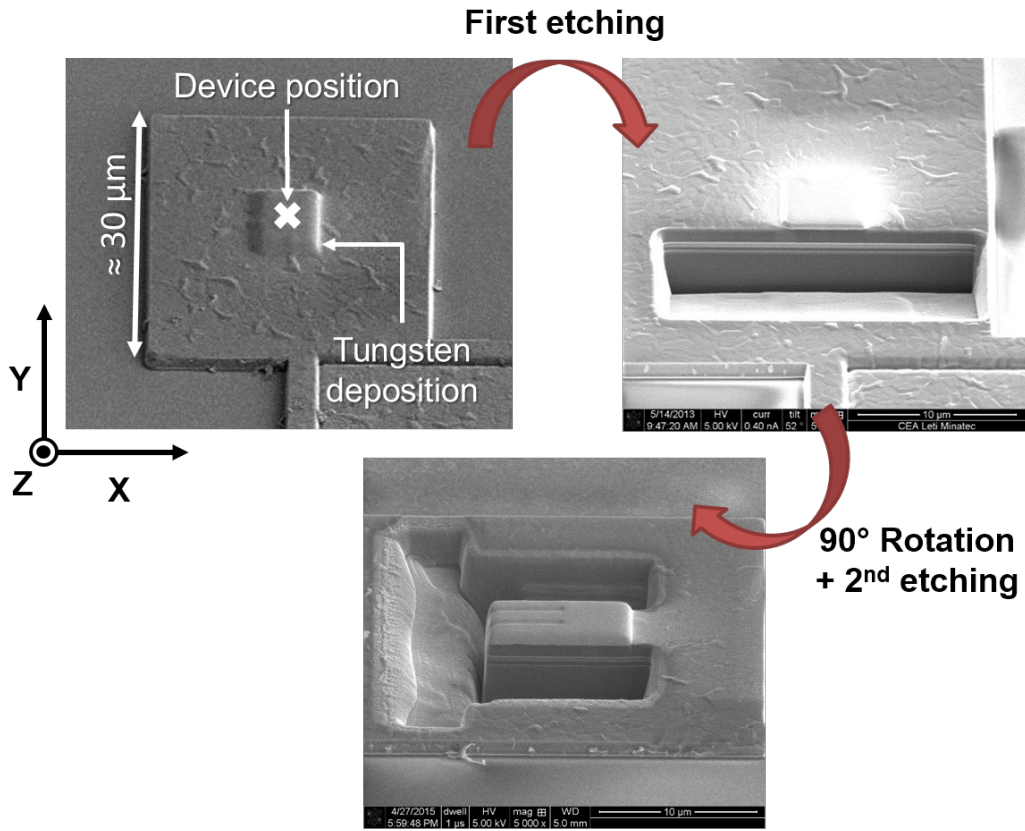


Figure 3.5: First steps of the FIB preparation, showing the milling of the wafer around the device.

Once the sample is soldered and the needle removed, we can proceed to the thinning of the chunk (fig.3.6). As said before, precautions must be taken during this step regarding the energy of the ion beam, to ensure that we don't alter the structure of the phase-change material. Therefore, energies above 8 keV are avoided until the end of the preparation, as we get closer to the device.

Thanks to SEM imaging, we can check the thickness of the sample as it is slowly thinned. the thinning is stopped when the sample reaches a thickness of ≈ 100 nm or lower, which guarantees good observations and a maximized signal during EELS analyses.

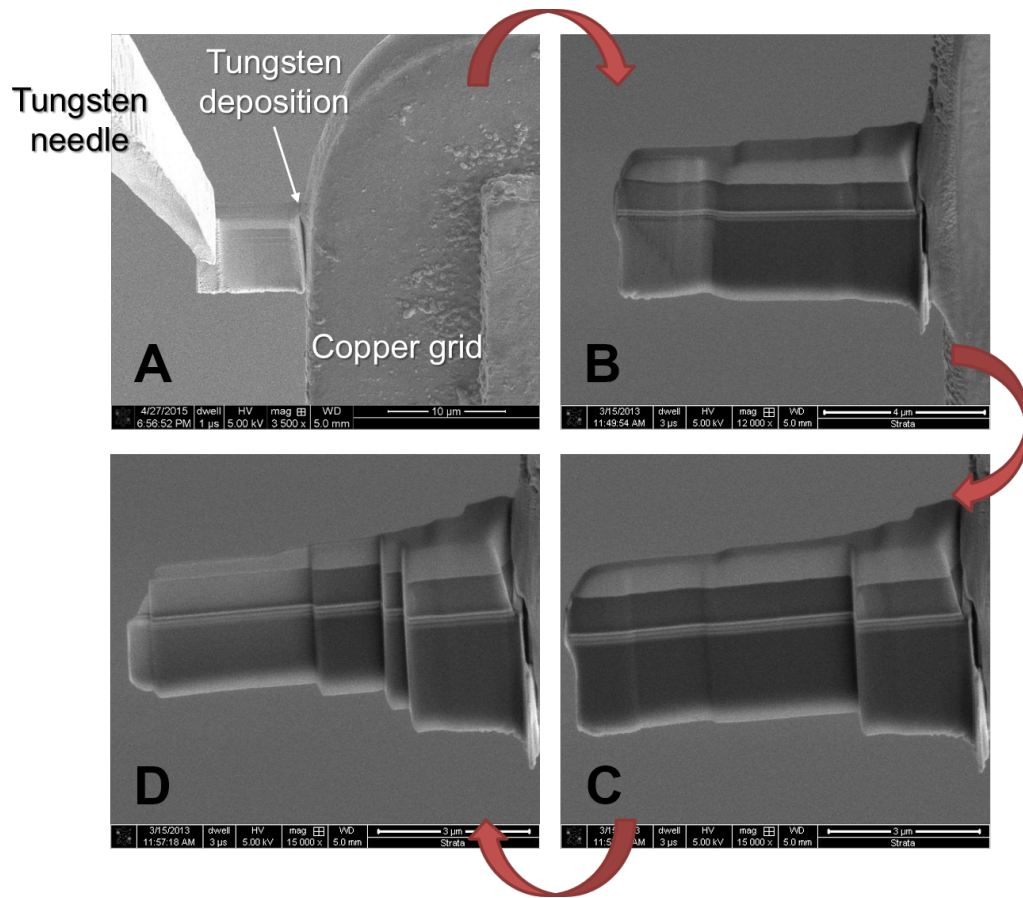


Figure 3.6: Soldering of the sample on the copper grid dedicated to TEM analyses (A) and final milling steps. The final sample shows a thickness of maximum ≈ 100 nm (D).

3.1.3 Avoiding Electrostatic Discharges

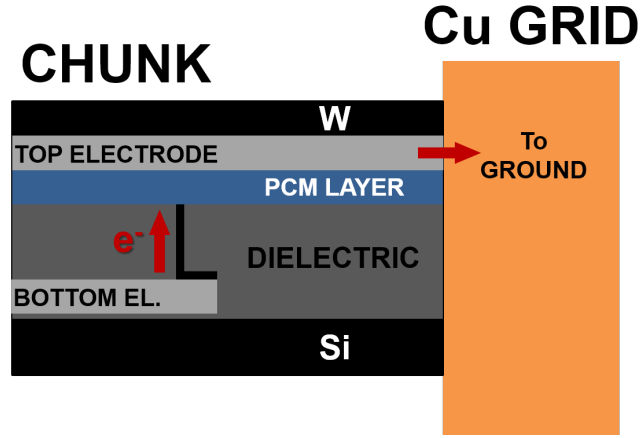


Figure 3.7: Schematic of the chunk fixed on the copper grid, showing that the electrons arriving on the bottom electrode because of SEM imaging can only escape through the heater.

As we said above, SEM imaging during the FIB preparation can cause the destruction of the cell because of ESDs. Indeed, the electrons arriving on the sample from the SEM beam must find a way out of it to be evacuated. But the structure of the device and the previous millings implies that the electrons sent on the bottom electrode can only escape by passing through the heater, as depicted in fig.3.7. This becomes an issue during the last steps of the preparation, as the heater gets thinner and thinner: if too many electrons arrives on the bottom electrode, a large voltage bias can appear across the heater, resulting in a sudden rise of temperature, melting of the materials, and hence the destruction of the device. Several samples were destroyed because of this effect during the first test campaign. Fig.3.8 shows two TEM images of such failures.

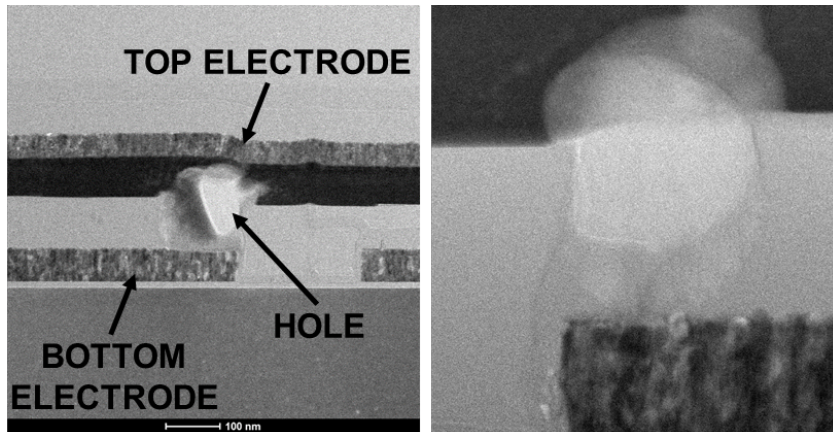


Figure 3.8: TEM images of the devices destroyed because of ESDs. The heater and its vicinity have melted, leaving a whole instead.

On these images we can clearly see the hole created by the electrostatic discharge during the FIB preparation. The heater has been destroyed, and its vicinity has melted, forbidding any further analyses.

This issue caused the loss of about 50% of the first test samples, forcing us to find a reliable solution for the next samples. We solved this problem by connecting the two electrodes of the device with a tungsten bridge, deposited on the side of the chunk by ion beam assisted deposition (fig.3.9).

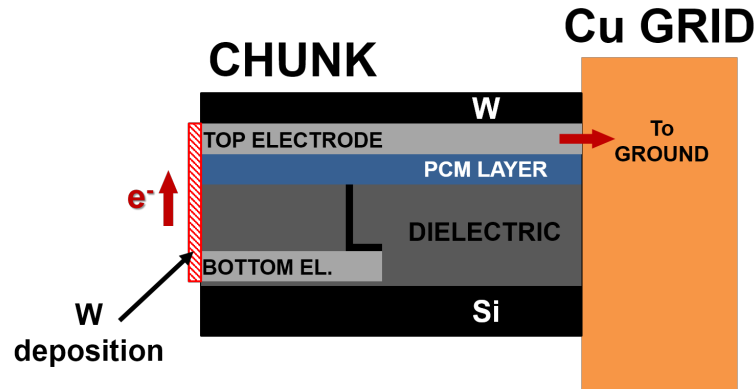


Figure 3.9: Schematic of the solution found to avoid ESDs in our samples. A tungsten bridge is deposited on the side of the chunk, connecting the two electrodes, thus allowing the electrons to evacuate the device.

This conductive bridge allows the electrons to evacuate from the bottom electrode without damaging the heater or the phase-change material. Fig.3.10 shows SEM images of the tungsten deposition made on the chunk. After we found this solution, no more damaged caused by ESDs were observed in our samples, which enabled us to conduct the morphological analyses of our devices.

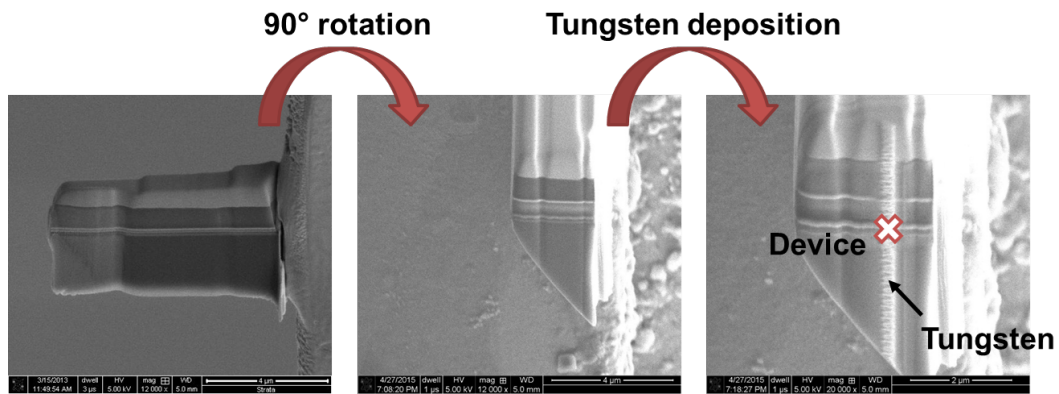


Figure 3.10: SEM images of the tungsten bridge deposited on the side of the chunk to evacuate the electrons from the bottom electrode to the top electrode.

After the FIB preparation, the samples underwent a last cleaning step in a plasma cleaner. Indeed, when the samples are taken out of the FIB instrument,

they are exposed to carbon contamination from the outside environment. If not removed, the carbon atoms segregate on the surface of the sample under the electron beam, inside the TEM. This would result in the degradation of the image during observations, but the plasma ($H_2 + O_2$) inside the plasma cleaner removes this contamination by creating C-O bindings with the carbon free radicals.

3.2 Results

Here we present the results of the TEM analyses performed on our GST + Ge45% + N4% devices. Transmission Electron Microscopy allows to observe of the cells at various scales, with magnifications ranging typically from 10 000 x up to 1.5 Mx in our case. It was thus a perfectly adapted characterization technique to investigate on the phenomena that we were interested in. A description of the TEM instrument, as well as the principles of TEM imaging and EELS acquisitions are given in appendix C. These analyses have been performed on two microscopes: a FEI Titan for the acquisition of images and diffraction patterns, and a FEI Tecnai Osiris for the acquisition of Electron Energy Loss Spectroscopy (EELS) maps. Both microscopes have been operated at 200 keV of beam energy. The images (bright field and dark field) and the diffraction patterns gathered enable us to study the structure of the phase-change material, while EELS maps give us information on the spatial distribution of elements inside the cells. Some of the devices presented in the beginning of this chapter are not reviewed here, because they exhibited very similar results to the ones we chose to show. Hence, only one RESET, std SET and SETMIN devices will be presented in this section.

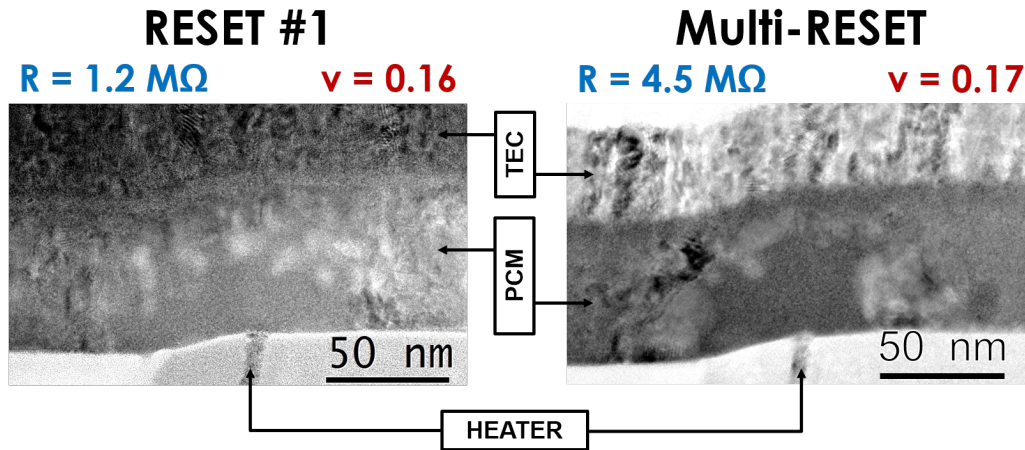


Figure 3.11: Bright Field images of the RESET and Multi-RESET devices showing the PCM layer in the vicinity of the heater. The contrasts seen between the area above the heater and the rest of the surrounding material evidences the difference of structure between those two zones, suggesting the presence of amorphous material inside the AV, surrounded by crystalline grains.

3.2.1 RESET & Multi-RESET

For the study of the high resistance states of the Ge-rich cells, we will show the results obtained on the RESET #1 and Multi-RESET devices introduced earlier. Fig.3.11 displays Bright Field (BF) images of the region of interest in both devices, i.e. the region of the phase-change material which is affected by the electrical pulses, which we will refer to as the Active Volume (AV). The resistance R and drift coefficient ν values are also given as a reminder. On both devices, we can see a difference of contrast between the zone near the heater and the rest of the PCM layer, attesting a change of the material structure in this dome-shaped volume. A closer view of the AV and its periphery (fig.3.12) suggests that the atoms inside the AV are in an amorphous phase, because of the blurred disks obtained by the FFT. Outside the AV, the FFTs exhibit bright spots, suggesting the presence of crystalline planes in the surrounding material.

Consequently, Dark Field (DF) images and Diffraction Patterns (DPs) have been acquired in order to get more information about the crystallinity of the AV and the rest of the PCM layer (fig.3.13 and 3.14). As described in appendix C, DF images enable to highlight the crystalline grains or the presence of amorphous zones in the material, and nanobeam DPs allow us to determine the crystalline structure of the grains.

The results show that the inside of the AV above the heater is amorphous, as expected, while the periphery of the AV exhibits crystalline grains of various sizes and orientations, but always in cubic configuration. Note that the resolution of the nanobeam DPs does not allow us to distinguish the cubic phase of GST compounds from the cubic phase of pure germanium, which both present a very similar diffraction pattern. Spectroscopy techniques like EELS are therefore useful to complete our study, since they can give information about the spatial distribution of chemical elements inside the PCM layer.

The spatial distribution of germanium, antimony and tellurium was studied by acquiring EELS maps covering the AV and its vicinity. These maps are obtained by acquiring EELS spectra point by point as we scan the sample with the electron beam, each map containing approximately 5000 points (50 x 100). For each point, 5 EELS spectra have been acquired and averaged. The averaged spectra collected on each point are then processed using Hyperspy, a powerful python-based multi-dimensional data analysis toolbox, which enables to smoothen the data by eliminating the high frequencies components of the signals [de la Pena 2015]. Once all the collected spectra have been processed with Hyperspy, we can proceed to the construction of the maps. First, the edges corresponding to Ge (1217 eV), Sb (527 eV) and Te (577 eV) are identified (fig.3.15).

Then, we measure the area (integrated intensity) of each edge by subtracting the background signal. Great care is taken during this step to avoid any artifact or miscalculation, especially concerning antimony and tellurium which present very close edges. An example of background removal for the antimony edge is given in fig.3.16.

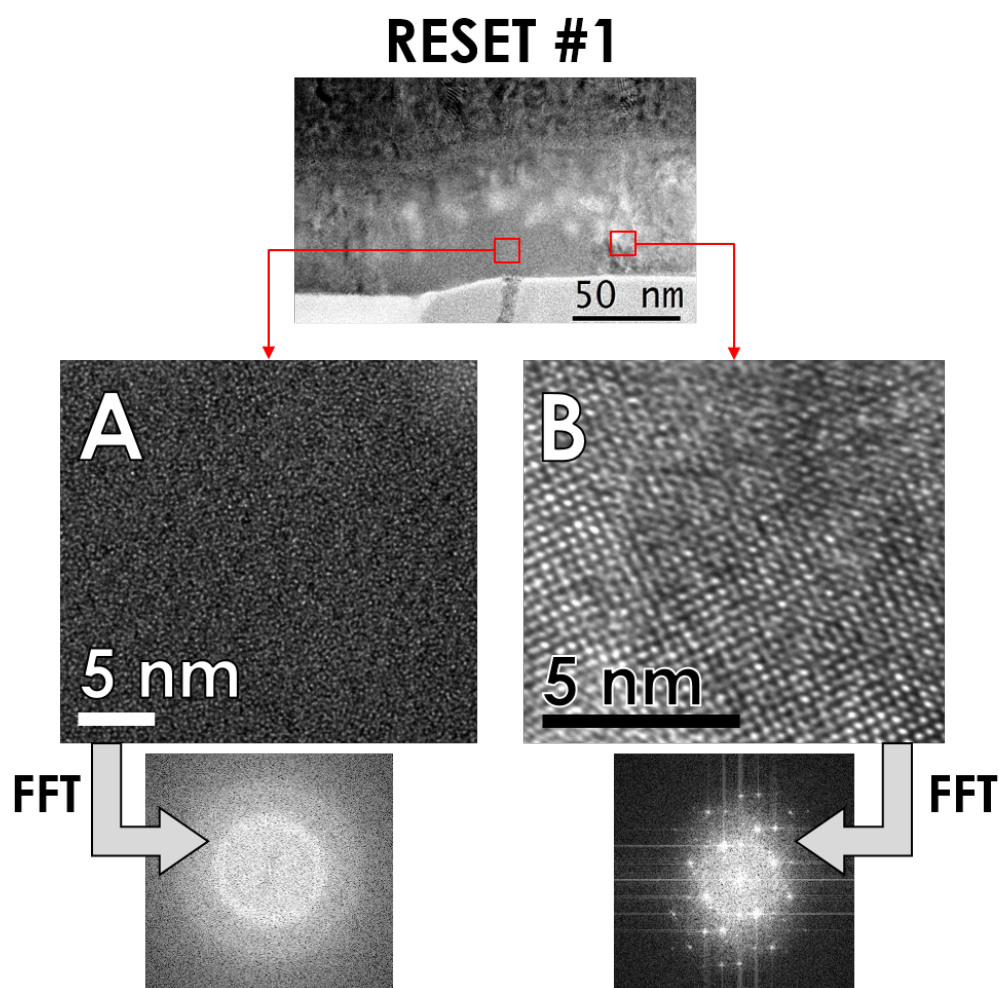


Figure 3.12: Close-up view of the inside of the RESET #1 AV (A) and its periphery (B). No particular order can be seen in (A) while atomic columns are observed in (B). The Fast Fourier Transformations (FFTs) performed on (A) exhibit blurred disks typical of amorphous material, whereas the bright spots seen in the FFT of (B) confirm the presence of crystalline planes.

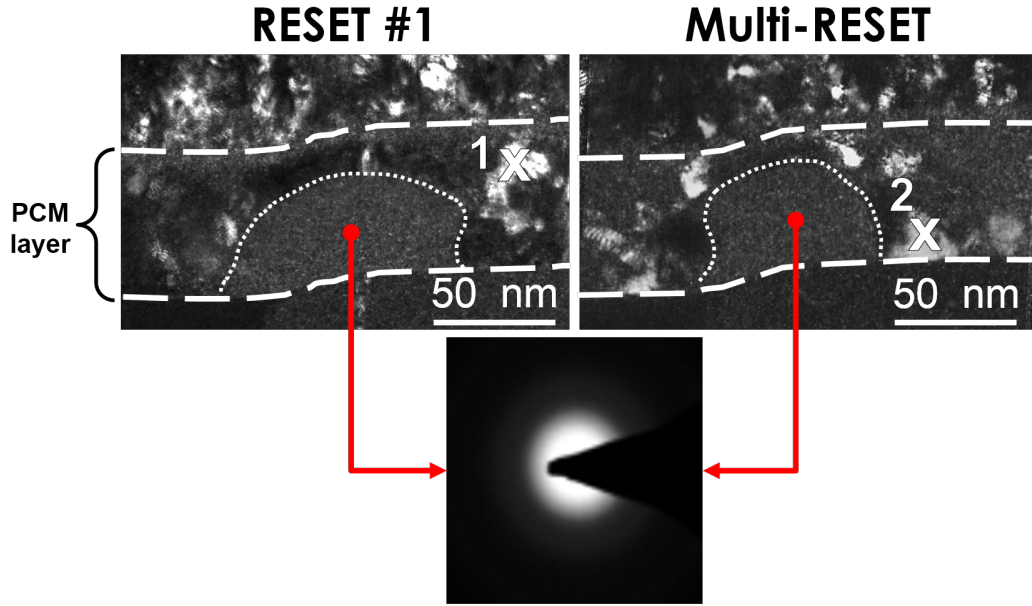


Figure 3.13: Dark Field images of the RESET and Multi-RESET devices. Crystalline grains are highlighted outside the AV, while the diffraction patterns acquired inside of it confirm the presence of amorphous material. The positions 1 and 2 marked on the images correspond to the position of the beam for the acquisition of the nanobeam DPs shown in fig.3.14.

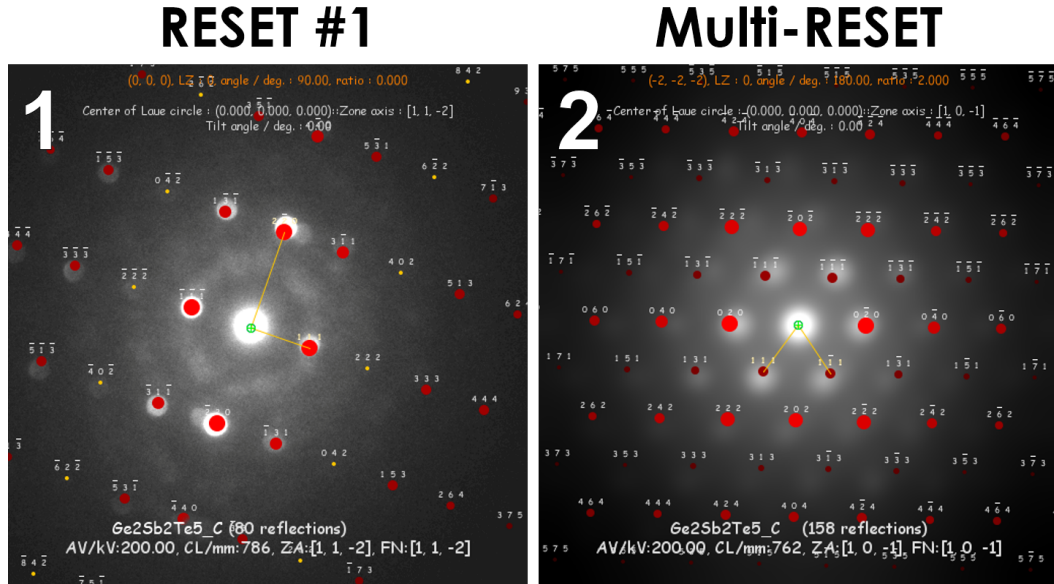


Figure 3.14: Nanobeam diffraction patterns acquired outside the AV of the RESET and Multi-RESET devices. The indexing of the patterns allow us to identify the crystalline structure of the grains highlighted in the DF images, which are found to be in cubic configuration [JEMS 2015].

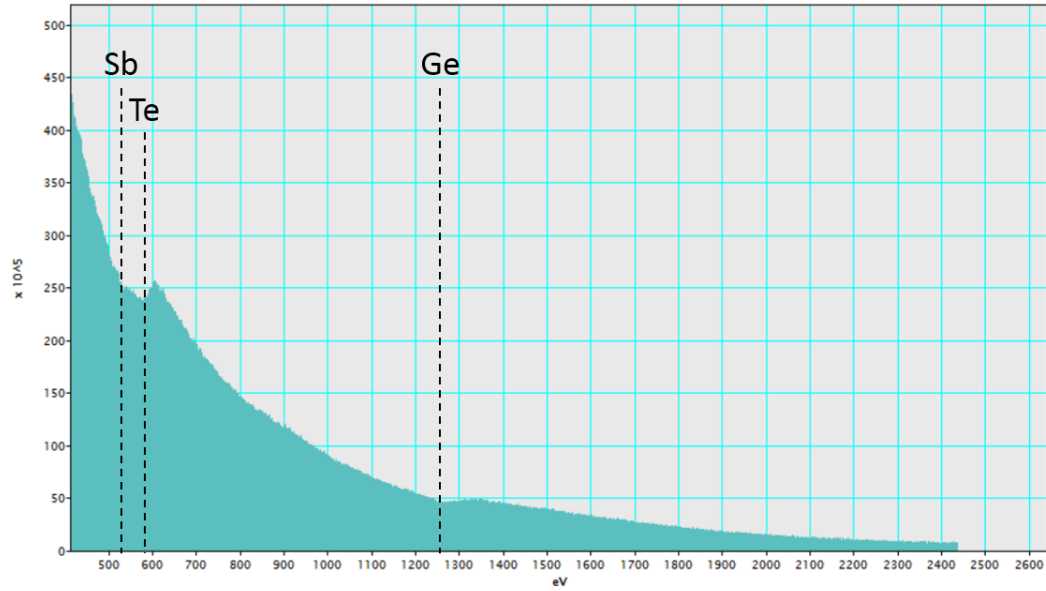


Figure 3.15: Example of an EELS spectrum acquired in the PCM layer of a test sample. The edges corresponding to Ge (1217 eV), Sb (527 eV) and Te (577 eV) are identified.

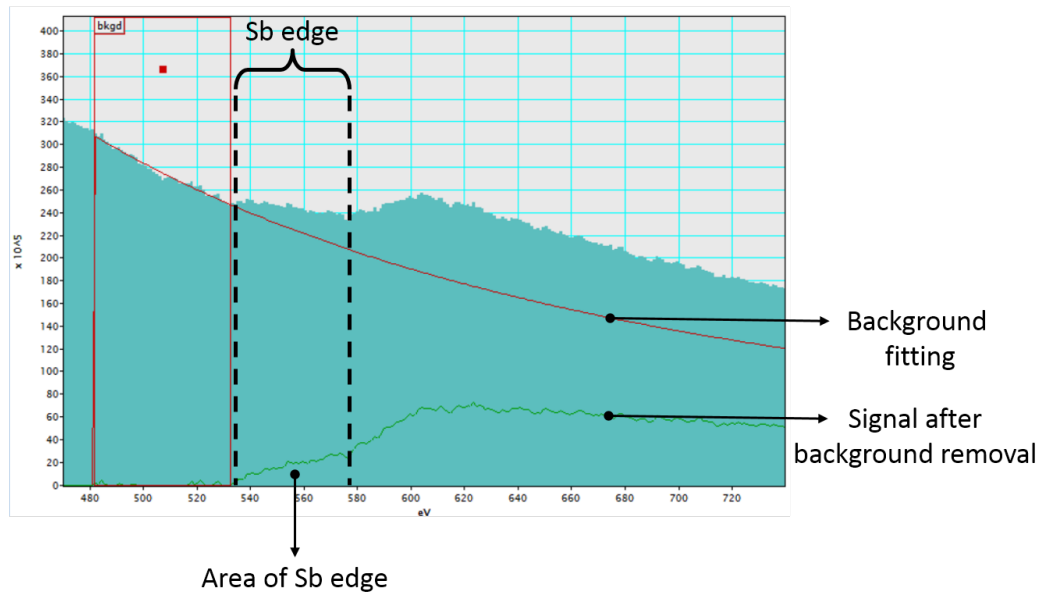


Figure 3.16: Example of a background removal to measure the area of the Sb edge.

This method is applied to each element, for each point of the map, giving qualitative information about the distribution of elements in the PCM layer. The results obtained on the RESET #1 and Multi-RESET devices are shown in fig.3.17. Note that these maps represent the spatial distribution of one element relatively to itself. This means that we cannot compare the intensities measured in the Ge map with the intensities of Te for example (i.e. we cannot say, at the moment, if there is more Ge than Te in a particular position).

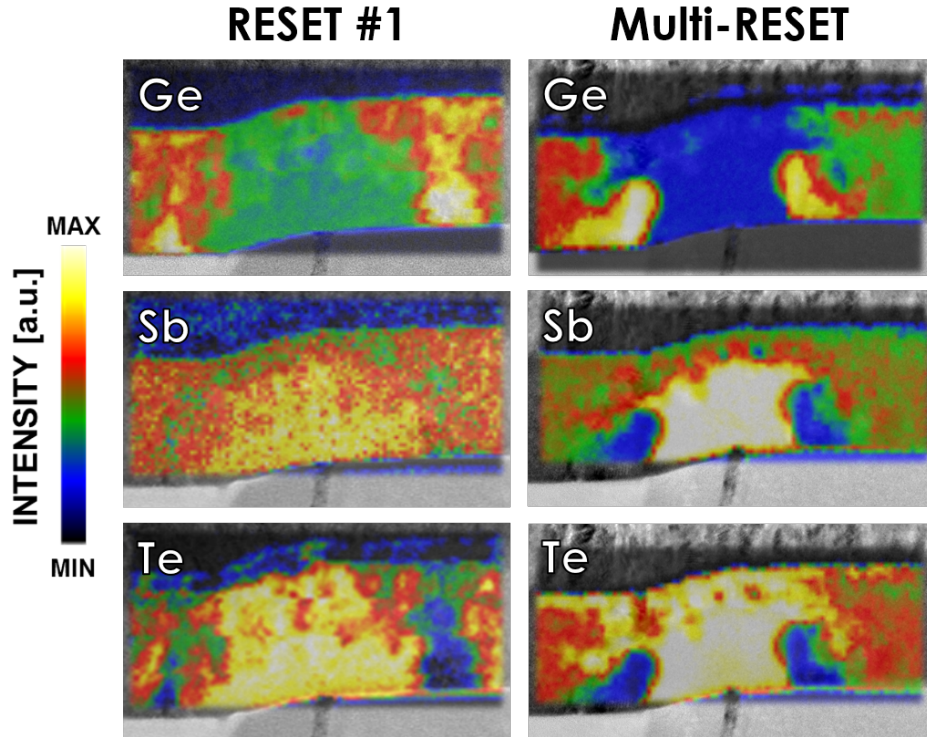


Figure 3.17: EELS maps of the RESET & Multi-RESET devices (superimposed on bright field images). Germanium is partially expelled from the active zone while antimony and tellurium migrate towards it.

From these maps, we can see that atomic migration is observed in both devices: Ge is partially expelled from the AV, creating Ge rich regions outside the amorphous area; Sb and Te moved in the opposite way, towards the inside of the AV, leaving the Ge-rich regions at the edge of the AV. Comparing EELS maps and dark field images, it appears that these Ge-rich regions are crystalline, while the pattern formed by the Sb and Te migrations inside the AV matches the shape of the amorphous area.

3.2.2 Standard SET & SETMIN

Unlike the RESET and Multi-RESET, the BF images of the SET & SETMIN devices programmed in a low resistive state do not display any dome-shaped pattern (fig.3.18). The close-up views of each cell's AV and their respective FFTs show

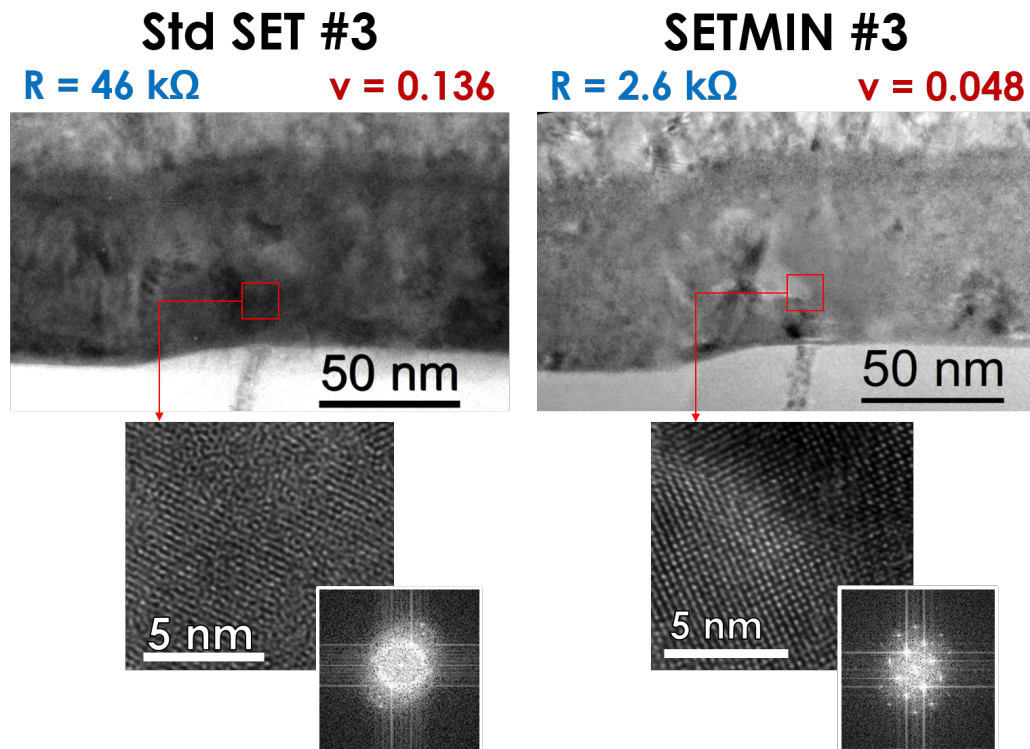


Figure 3.18: Bright Field images and FFTs of the SET and SETMIN devices. No dome-shaped pattern is observed, the AV of both devices seem to be crystalline, with still some signs of amorphous material in the standard SET cell.

that crystalline grains have been formed in both devices, but they also suggest the presence of amorphous residues in the AV of the standard SET cell, as if the recrystallization of the material was incomplete in this device.

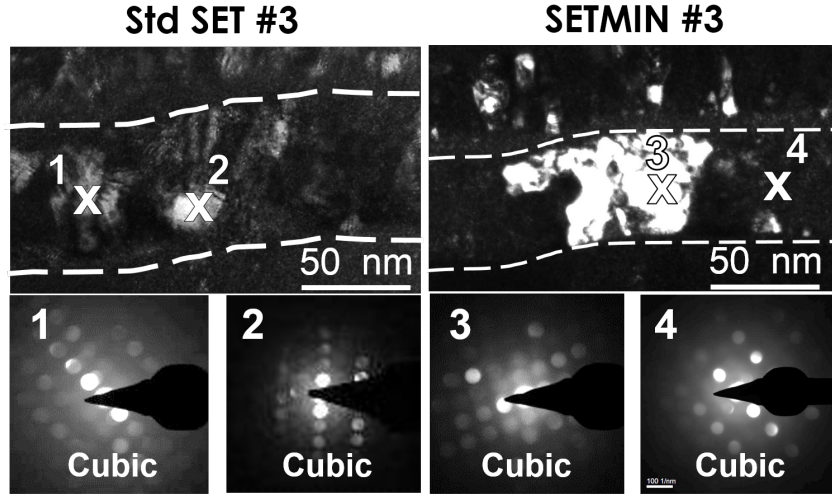


Figure 3.19: Dark Field images of the SET and SETMIN devices. A crystalline structure extends over the full PCM layer thickness in the SETMIN cell, from the heater to the top electrode, while smaller crystalline grains are observed in the standard SET.

The dark field images (fig.3.19) confirm that crystalline grains have been created in the AV of the two devices, with smaller grains in the AV of the SET cell with respect to the ones observed in the SETMIN cell: in the latter, a crystalline structure of single orientation and much larger size than the other surrounding crystalline grains extends over the entire thickness of the PCM layer from the heater to the top electrode. Concerning the SET device, the crystalline grains inside the AV do not show a clear difference in size from the surrounding grains. A diffraction pattern of a larger area of the standard SET's AV has also been acquired (fig.3.20), confirming the formation of crystalline grains, but also the presence of amorphous material in this cell. Once again, all the crystalline grains analyzed by diffraction have been found to be in cubic phase.

The EELS maps acquired on those devices (fig.3.21) reveal the same migration behavior as the one observed in the RESET and Multi-RESET devices, with concentration of antimony and tellurium inside the AV while germanium is concentrated at its borders. Notice that in the SETMIN sample, the segregation pattern matches the shape of the crystalline structure inside the AV.

3.2.3 R-SET

The R-SET devices (fig.3.22 and 3.23) exhibit a more peculiar structure than the previous devices. Indeed, the BF images suggest that the phase-change material is in a crystalline configuration in the center of the AV, surrounded by two zones of amorphous material. The R-SET B #1 cell differs from the other R-SET devices,

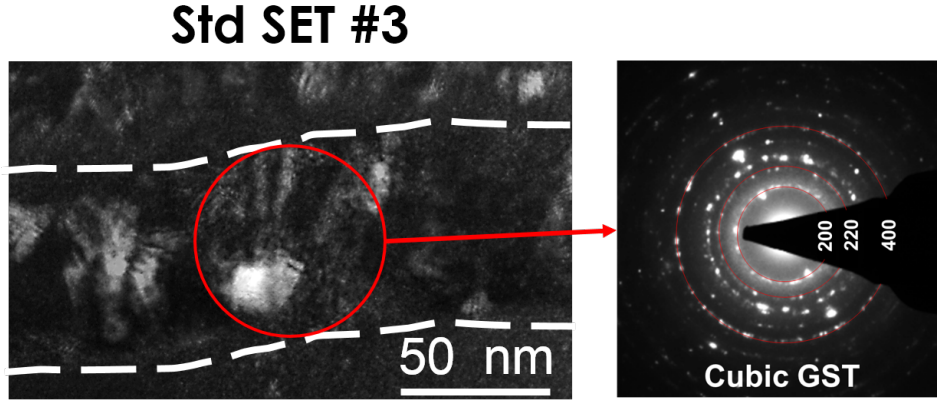


Figure 3.20: Diffraction pattern (right) of the area circled in red on the DF image (left) of the standard SET device. The circles attest the presence of crystalline grains, while the blurred disks confirm the presence of amorphous material.

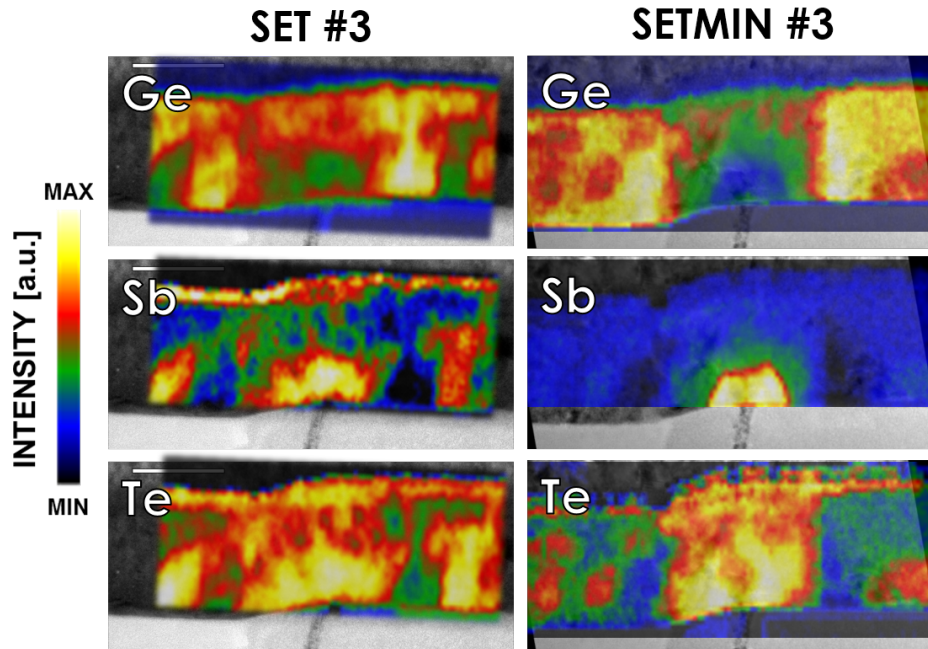


Figure 3.21: EELS maps of the SET & SETMIN devices.

with evidences of a void formation above the heater, hence explaining the higher resistance of the device with respect to the other R-SET cells.

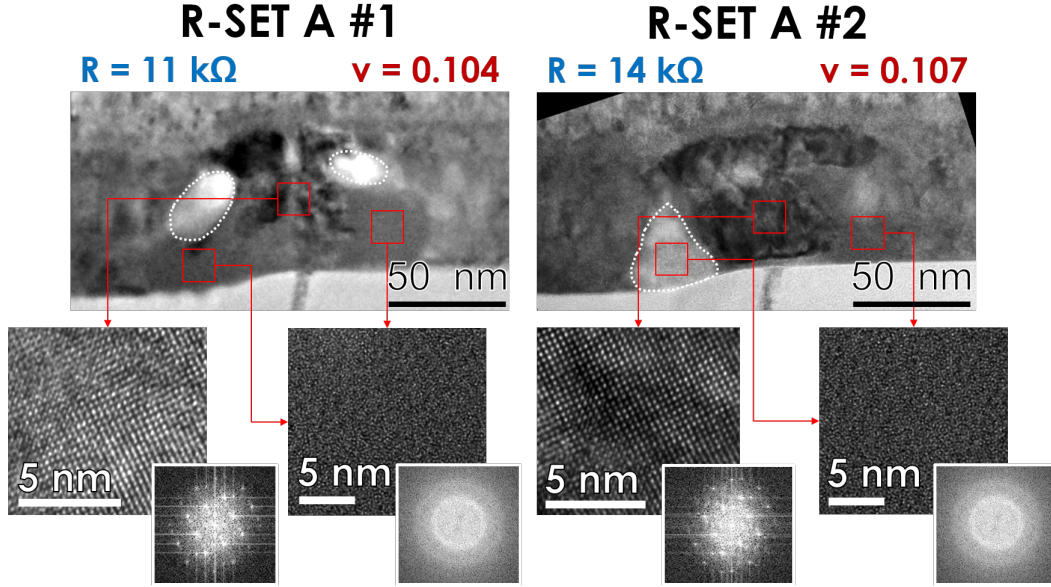


Figure 3.22: Bright Field images of the R-SET A #1 and #2 devices. The small areas circled in white correspond to low density regions, evidencing the formation of voids in the periphery of the AV. Close-up views show that the phase-change material inside the AV of the two devices exhibit both ordered and disordered atomic arrangement, with crystalline planes present in the center, surrounded by two regions of disordered material.

The Dark Field images of these devices (fig.3.24 and 3.25) reveal that their AV contains a crystalline structure very similar to the SETMIN cell, crossing the PCM layer and connecting the heater to the top electrode. But this crystalline path is surrounded by two amorphous regions (except in the R-SET B #1 device), similar to the ones observed in the RESET cells. The diffraction patterns confirm the amorphous nature of these regions, and show that the crystalline grains created in the center of the AV are in a cubic configuration.

The most important difference between the R-SET A and the R-SET B samples comes from the small PCM region in contact with the heater. In the R-SET B devices, this region hasn't been fully recrystallized, as shown in fig.3.26, whereas the crystalline grains are really contacting the heater in the R-SET A cells.

Concerning the spatial distribution of elements, we observe once again the depletion of germanium above the heater and the concentration of antimony and tellurium (fig.3.27 and 3.28). As in the previous devices, Ge-rich regions are created at the periphery of the AV in both cells.

3.2.4 GST 225

To complete this study, and more specifically to understand the germanium impact on atoms displacement in the PCM layer, another device integrating pure GST (i.e.

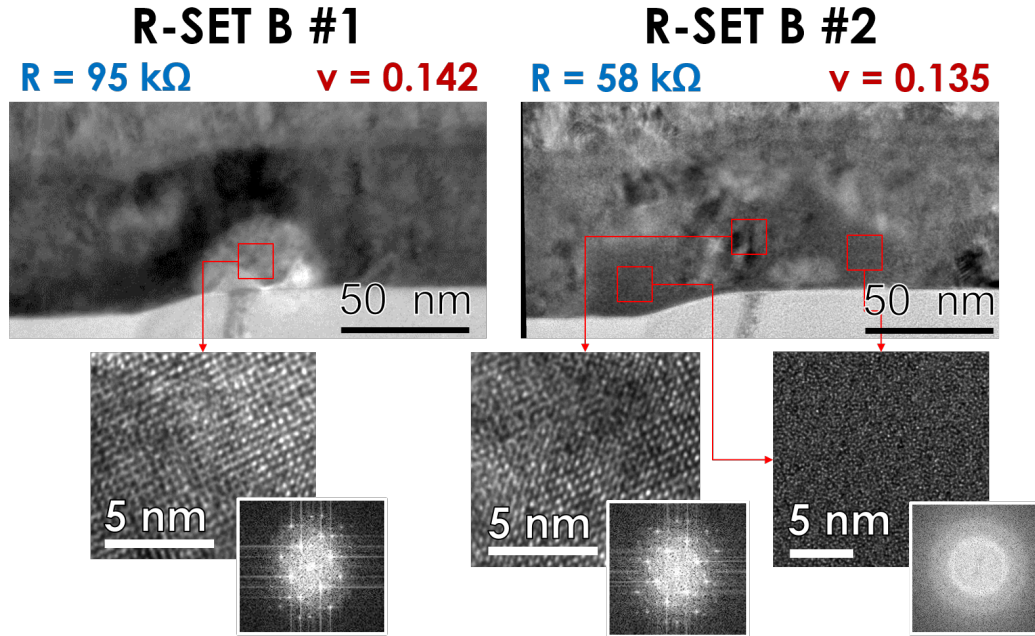


Figure 3.23: Bright Field images of the R-SET B #1 and #2 devices. The area circled in white above the heater of the R-SET B #1 cell correspond to the formation of a void, thus explaining the high resistance. As in the R-SET A devices, close-up views evidence the presence of both ordered and disordered atomic configurations inside the AV.

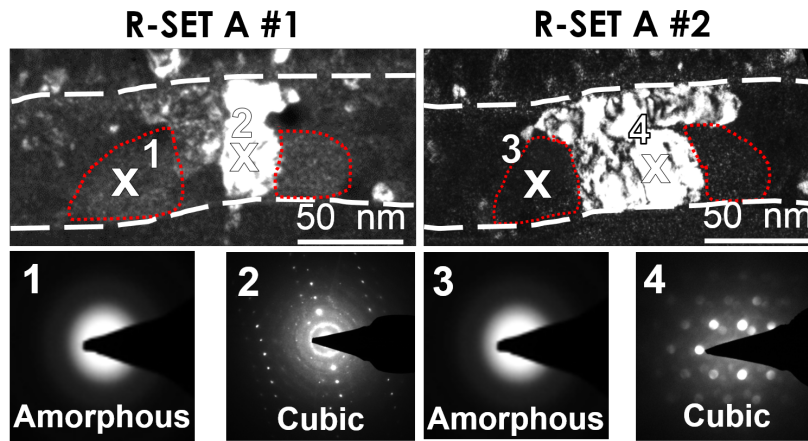


Figure 3.24: Dark Field images and Diffraction Patterns of the R-SET A devices. A SETMIN-like crystalline structure of cubic configuration is observed in the middle of the AV, connecting the heater to the top electrode. This crystalline path is surrounded by two RESET-like amorphous zones, circled in red.

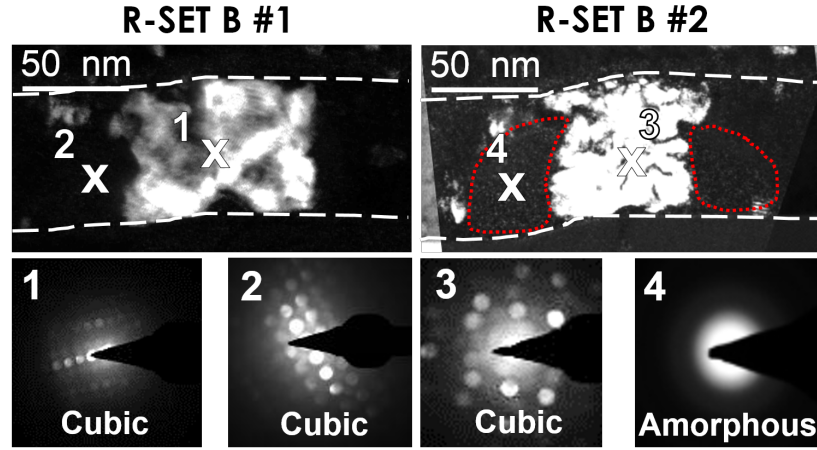


Figure 3.25: Dark Field images and Diffraction Patterns of the R-SET B devices, evidencing the formation of a crystalline structure of cubic configuration connecting the heater to the top electrode in both devices. In the case of the R-SET B #2 device, two amorphous regions are also visible (circled in red) on both sides of the crystalline path.

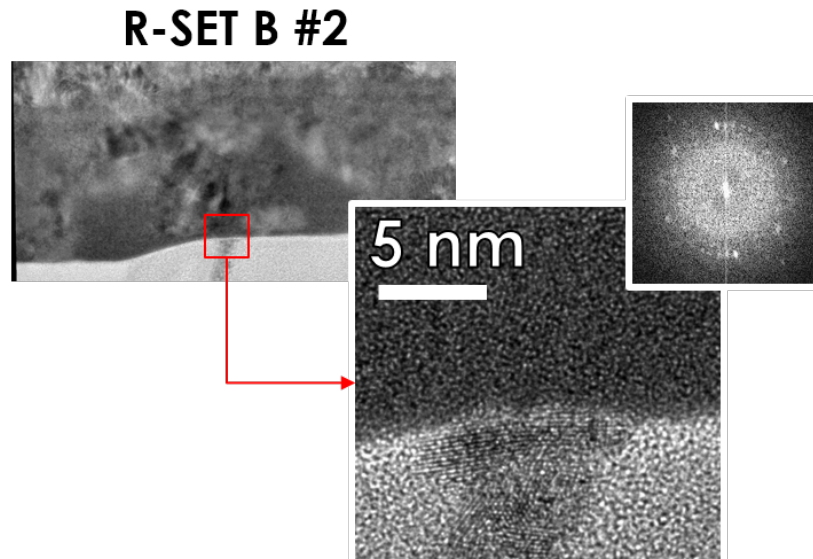


Figure 3.26: Close-up view of the contact area between the heater and the PCM layer in the R-SET B #2 device. Atomic disorder is evidenced in the phase-change material (the bright spots in the FFT image come from the crystalline planes present in the heater).

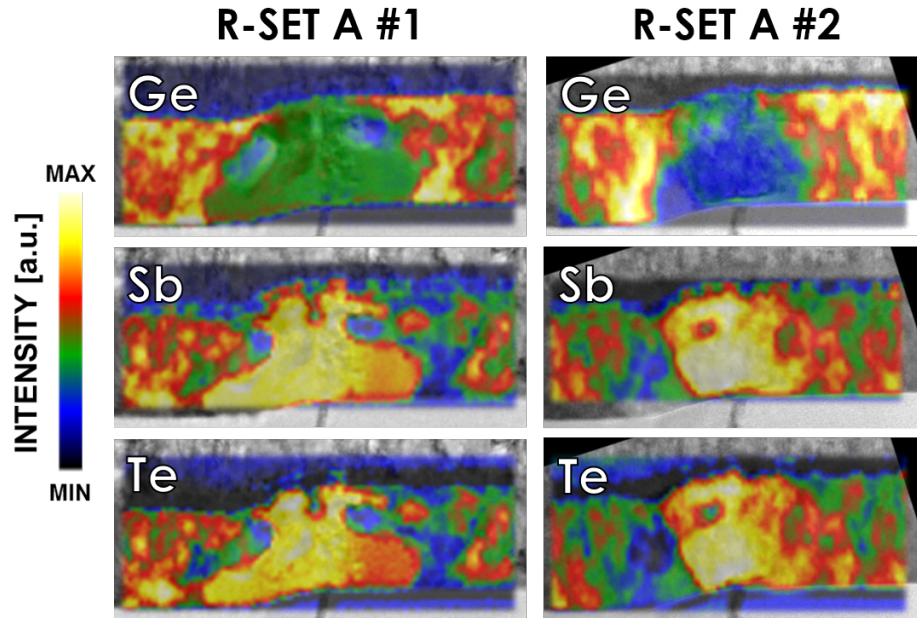


Figure 3.27: EELS maps of the R-SET A devices.

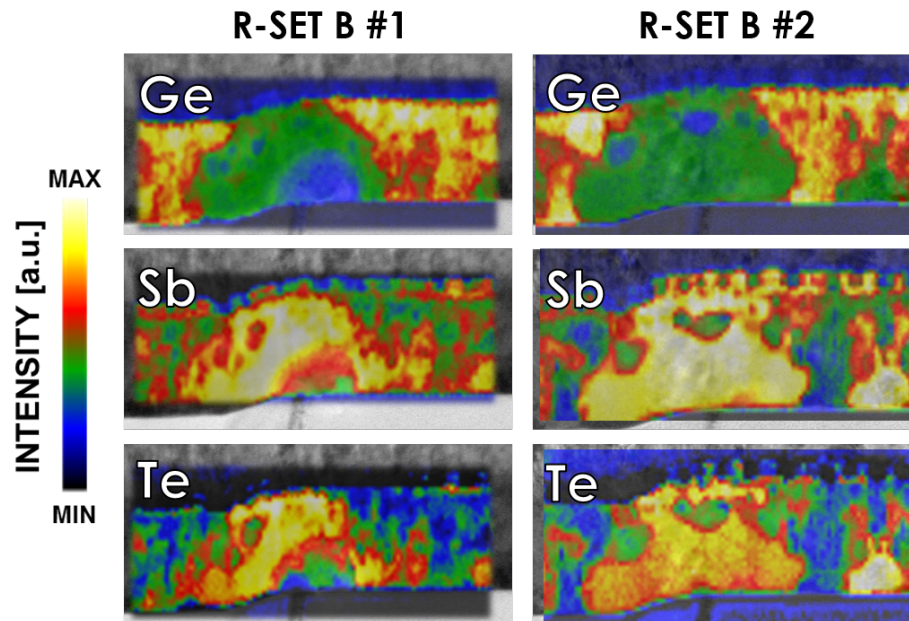


Figure 3.28: EELS maps of the R-SET B devices.

without germanium enrichment) was programmed in the SETMIN state and studied following the same analyses than the devices presented above.

GST - SETMIN

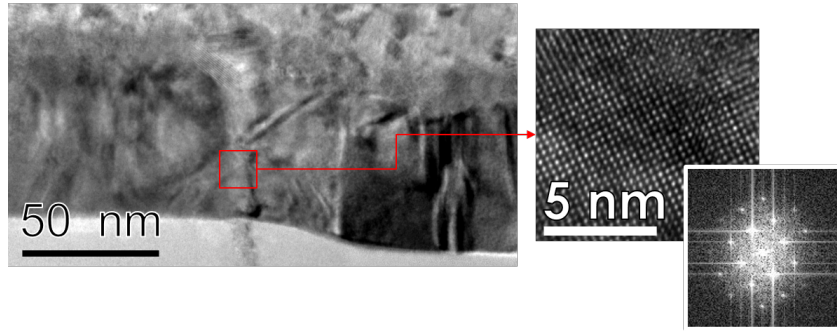


Figure 3.29: Bright Field images and FFT obtained on the GST -SETMIN device.

From the BF images (fig.3.29) we can already see that the material seems fully crystalline, the close-up view of the AV showing atoms arranged in crystalline planes. In fact, the structure of the phase change material revealed by the DF images (fig.3.30) is similar to the one observed in the Ge-rich SETMIN device: crystalline grains in cubic configuration have been formed above the heater, filling the entire AV and its vicinity. The structures observed in this cell are the largest observed from all the devices under test.

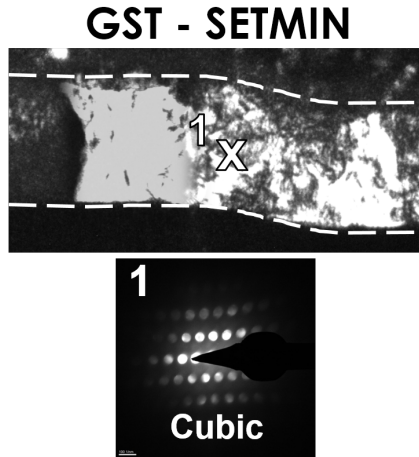


Figure 3.30: Dark Field images (two images superimposed) and nanobeam diffraction pattern of the GST-SETMIN device. Full recrystallization is observed.

The EELS map of this device shows the same migration of atoms as in the previous devices with Ge and Sb moving in opposite direction, except for Te which does not seem to concentrate inside the AV.

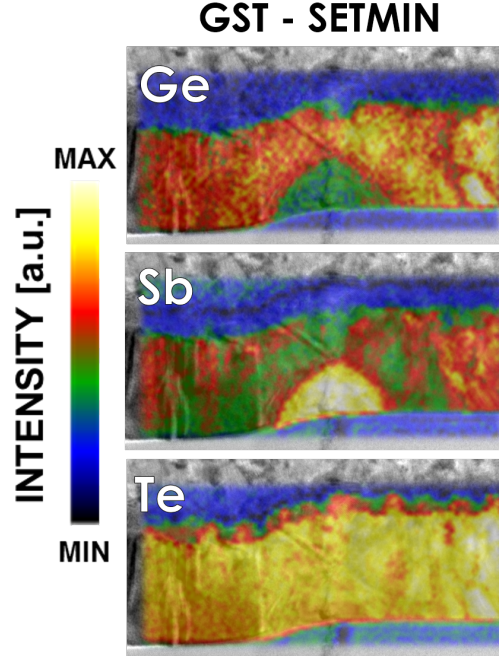


Figure 3.31: Results of the morphological and EELS analyses of the GST 225 device. Large crystalline grains are visible, and clear segregation of Ge and Sb is observed.

More information can be gathered on the segregation of elements in the PCM layer by performing quantitative analyses on the EELS spectra, which is the object of the next paragraph.

3.2.5 Quantitative analyses

Using the spectra collected in the EELS maps, quantitative measurements have been performed to analyze the composition of the AV in each device (refer to the appendix "TEM" for more information on quantitative analyses). As the EELS analyzes have been optimized for maps acquisition, the results of these quantitative measurements cannot reach an accuracy smaller than ± 5 at%. However, these analyzes give us important information about the concentration variations between the AV and the rest of the PCM layer.

From the EELS maps gathered on all samples, we can extract the spectra of specific areas and perform quantitative measurements on them. The average relative concentrations of germanium, tellurium and antimony in the PCM layer are first determined using all the spectra from the PCM area of the EELS maps (fig.3.32).

Despite the moderate accuracy of these quantifications, the results remain consistent with the nominal values (i.e. target compositions) used during the deposition process of the PCM material. These numbers are then compared to the concentrations measured inside the AV using only the spectra from this particular zone (fig.3.33).

Table 3.1: Results of the EELS quantitative analyses inside the AV of the GST device.

	Concentrations (at.%)		
	Ge	Sb	Te
Ref.	22	22	56
Whole layer	19 ± 8	19 ± 8	62 ± 5
AV	6 ± 8	32 ± 7	62 ± 5

For all devices, we notice a strong reduction of germanium concentration inside the AV. The difference of Ge content between the AV and the surrounding material varies from one device to another: the SETMIN device exhibits the strongest Ge depletion with a difference of 37 at% between the AV and the rest of the layer while this number stays around 20 at% for the other devices. Antimony and tellurium are affected in the same amount proportions, as their concentration rises inside the AV. The quantitative analysis performed on the GST-225 device (table 3.1) show the same tendencies, except for Te which is homogeneously distributed in the PCM layer.

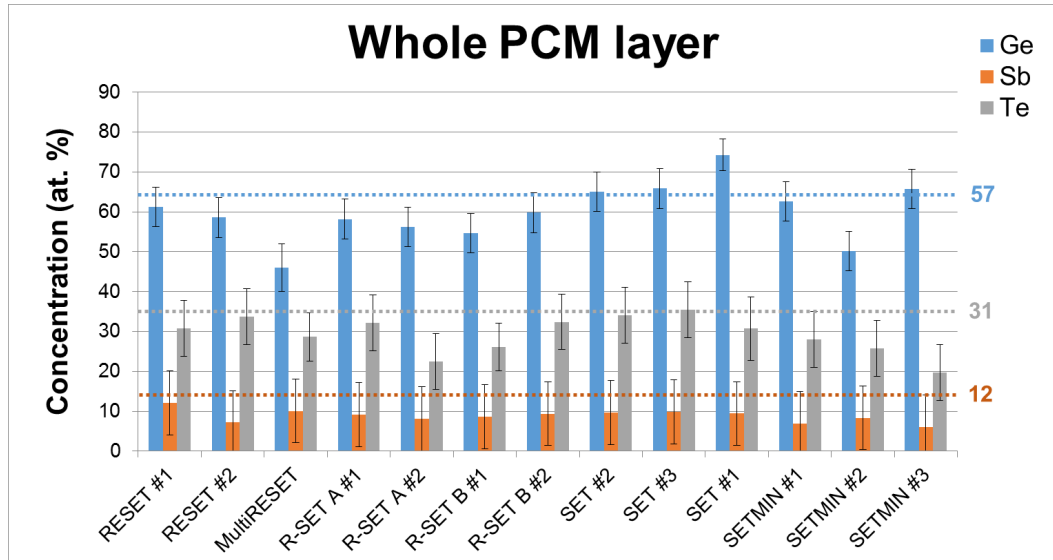


Figure 3.32: Histogram of the average concentrations of Ge, Sb and Te in the PCM layer of each device. The numbers on the right hand-side of the graph represent the reference concentrations, taken as the nominal compositions used during the deposition of the material.

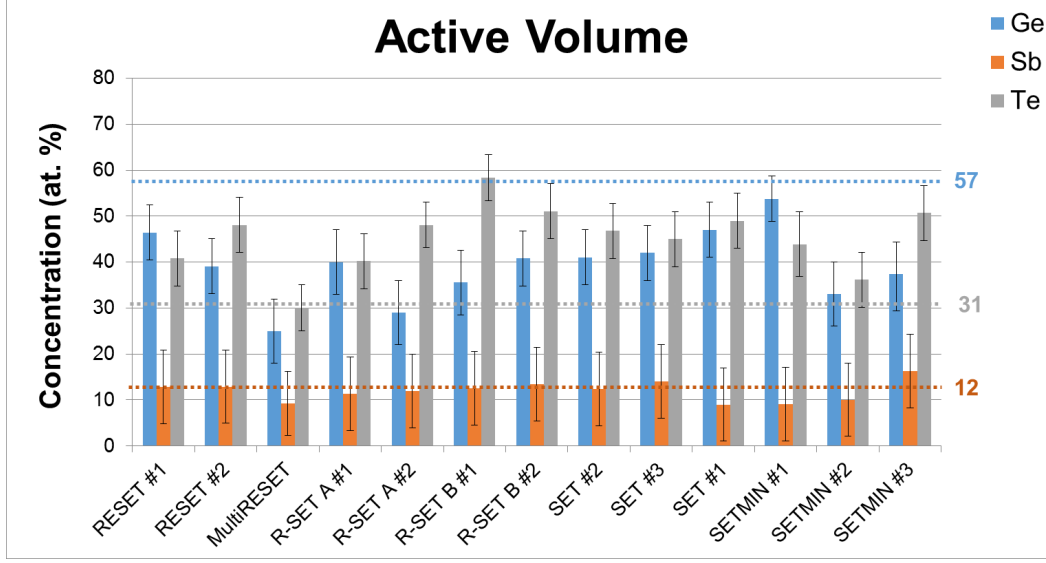


Figure 3.33: Histogram of the average concentrations of Ge, Sb and Te in the AV of the devices.

3.3 Simulations

The phase-change mechanisms implied during the SET operations of our devices have been simulated using a finite-volume electro-thermal solver coupled with the Level Set Method [Gliere 2011] (details of the equations used in this model are given in appendix D). In these simulations, the devices are initially in a RESET state, the PCM material in the AV being amorphous. The SET operation was simulated using both low and high current programming pulses (respectively 600 and 1000 μA), to reproduce the experimental programming using respectively an R-SET or a standard SET procedure. The simulated pulse comprises a plateau of 500 ns and a trailing edge of respectively 500 and 1000 ns. To take into account the increase of T_c in our Ge-rich GST cells, the nucleation rate and the crystalline growth velocity have been reduced with respect to pure GST. The simulations qualitatively reproduce the formation of a conductive filament where the material has switched from the off state to the on state. This switch leads to the heating of the surrounding material along the filament until melting, resulting in the creation of a melted domain inside the amorphous dome.

With the high current pulse (fig.3.34), the size of the melted region starts to decrease after 500 ns until its total disappearing at 800 ns, leaving the AV of the cell in a crystalline phase.

With the low current pulse (fig.3.35), the temperature field leads to the growth of the top crystalline material toward the inside of the amorphous dome. After approximately 360 ns a steady state is achieved, with only a small residual liquid volume remaining above the heater. This matches with the TEM images obtained on the R-SET B devices (fig.3.26) in which we saw that a small amount of PCM material remained amorphous above the heater. In the simulation, this little residue then

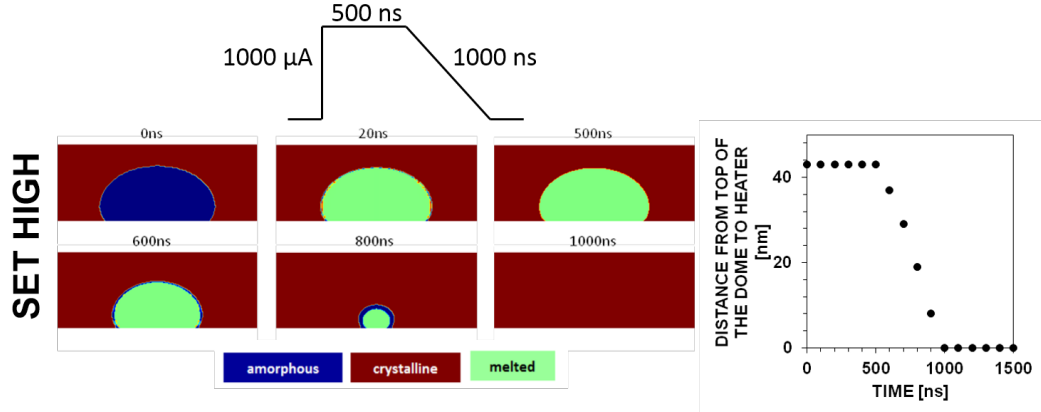


Figure 3.34: Simulation of the phase-change during the high current SET operation.

disappears during the first 25 ns of the trailing edge. The final image shows a crystalline column surrounded by two amorphous regions, which is in good agreement with the TEM observations of the R-SET devices.

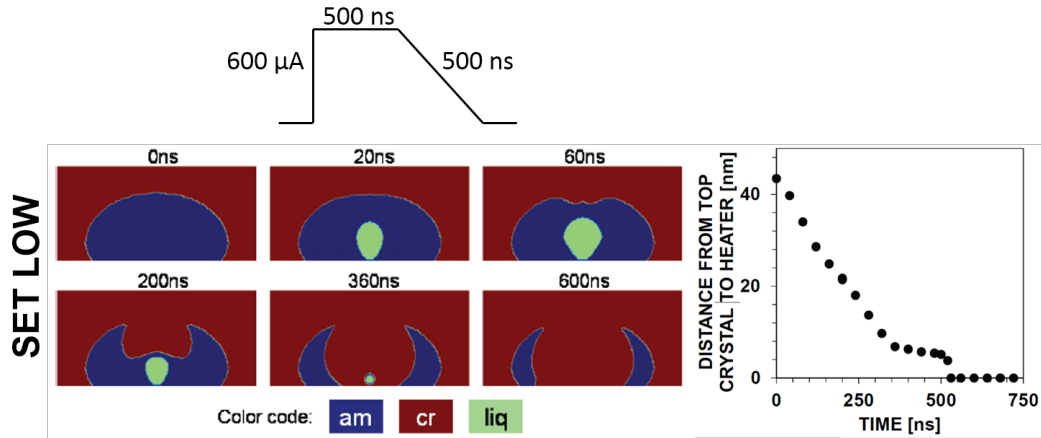


Figure 3.35: Simulation of the phase change during the low current SET operation.

3.4 Discussion

3.4.1 Morphological interpretation of the drift phenomenon

The morphological information gathered on all the devices, together with their electrical characteristics (resistance after programming & drift coefficient), enable to establish factual links between the drift phenomenon and the structure of the devices at the nanoscale. First, the electrical measurements presented in chapter 2 confirmed the dependence of the drift on the initial resistance of the cells [Kostylev 2008]: the higher the initial resistance, the stronger the drift. As said in the first chapter, debates are still open on the fundamental reasons causing this evolution of the re-

sistance over time, but studies have demonstrated the important role of structural relaxations inside the amorphous phase on the drift of the RESET states. Thanks to the TEM analysis presented in this chapter, we can bring new elements to the comprehension of the drift phenomenon in the SET states of Ge-rich devices. The morphological studies have indeed highlighted notable differences of crystallinity inside the AV of the cells programmed in a low resistive state: the SETMIN devices exhibit large crystalline grains, extending over the full thickness of the PCM layer and connecting the heater to the top electrode, which explains the good conduction of current and thus the low resistance measured. The crystalline grains observed in the AV of standard SET devices have been shown to be smaller, with residues of amorphous material also found between them, evidencing the incomplete recrystallization of the Ge-rich alloy in these devices (fig.3.36).

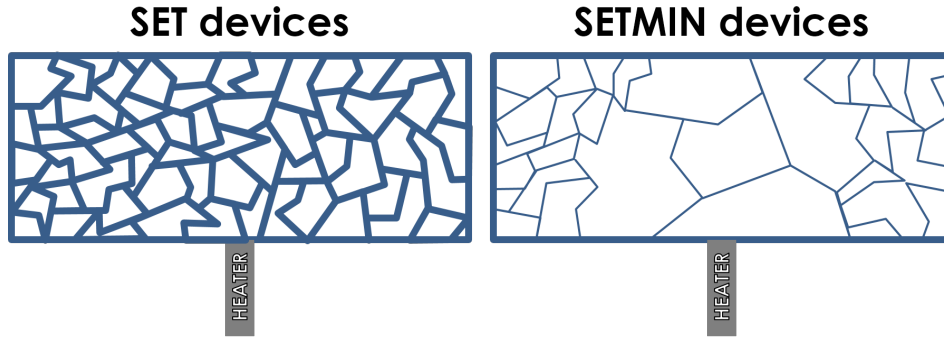


Figure 3.36: Schematic of the crystalline structure of the SET and SETMIN devices. The standard SET pulse is not able to fully recrystallize the AV of the cell, leading to the creation of smaller crystalline grains with respect to the SETMIN device, and to a larger amount of residual amorphous material at the grain boundaries.

This is the reason why the standard SET devices exhibit a higher resistance than the SETMIN devices: in the SETMIN cells, the large crystalline grains enable to create a good conduction path between the heater and the top electrode, while the numerous grain boundaries containing the residual amorphous material inside the SET's AV act like electronic barriers which need to be overcome. This also explain why the standard SET devices show higher drift coefficients than the SETMIN cells: the amorphous phase being subject to structural relaxations, then the device with the largest amount of amorphous material (i.e. the highest number of grain boundaries) will show the highest drift coefficient. But if we consider the R-SET devices, one can remark that this statement is not completely accurate: indeed, these devices exhibit a resistance and a drift coefficient smaller than the standard SET devices, despite a larger amount of amorphous material inside their AV. But just like in the SETMIN cells, the crystalline grains in the R-SET A's AV form a good conduction path between the heater and the top electrode (fig.3.37), while they are also larger than the ones observed in the standard SET devices. So this means that the drift phenomenon does not depend on the total amount of amorphous material inside the AV of the cells, but more specifically on the amount of amorphous

material on the conduction path between the heater and the top electrode. This also explains why the R-SET B devices are more resistive and exhibit higher drift coefficients than the R-SET A devices: without trailing edge, the pulse applied to the cell is not able to recrystallize the small region in the direct vicinity of the heater, thus leaving some amorphous material on the conduction path. Thanks to these results, we demonstrated that the drift phenomenon highly depends on the size of the crystalline grains which create the conduction path between the heater and the top electrode (i.e. larger grains lead to smaller drift). We can then optimize the electrical pulses to achieve even a partial recrystallization, but targeting large grain sizes. The procedure used to program the SETMIN device is the most efficient way to achieve this: by applying a series of relatively long pulses (50 pulses, $1\ \mu\text{s}$ each) with decreasing voltages to the cell, we allow the PCM inside the AV to recrystallize slowly, and we optimize the fraction of crystalline material formed inside the device at the end of the programming. The R-SET procedure also enables us to reach lower resistance and drift values than the reference SET states, but is much less time consuming than the SETMIN staircase down. By designing and experimenting new types of electrical programming, it is then possible to lower the drift of the cells.

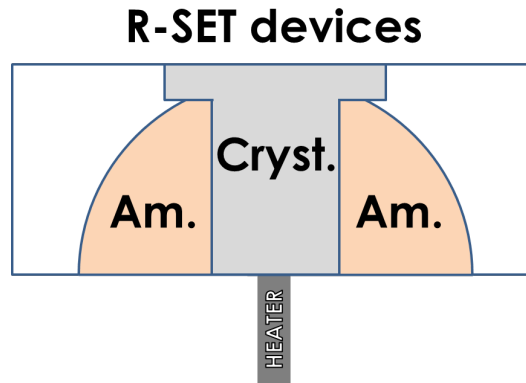


Figure 3.37: Schematic of the structure of the R-SET devices, showing the crystalline path enabling the conduction of current, crossing the amorphous dome created during the RESET pulse.

3.4.2 Concentration of elements and retention of the RESET state

Material characterization and electrical testing of the Ge-rich devices have demonstrated the improvement of the amorphous phase stability with increasing germanium content, showing a higher crystallization temperature than standard GST, thus leading to a better retention of the data. However the XRD measurements have revealed the formation of cubic germanium at 400°C , exhibiting the first signs of phase heterogeneities inside Ge-rich materials when temperature rises. Thanks to the EELS maps performed on the devices integrating these materials, we demonstrated that the heating of the cells by an electrical pulse with enough energy also

led to elemental heterogeneities inside the devices. All the maps presented in this study show the concentration of antimony and tellurium inside the AV just above the heater, while germanium is expelled toward the edges of this region (fig.3.38). These migrations are attributed to a segregation effect occurring during the RESET operation where strong temperature gradients are created inside the cell. Along the conductive path between the heater and the top electrode the temperature is high enough to melt the material. However at the periphery of this liquid zone, lower temperatures allow the solidification of germanium in the 640-920°C range while still in equilibrium with a Ge-impoverished GST liquid phase.

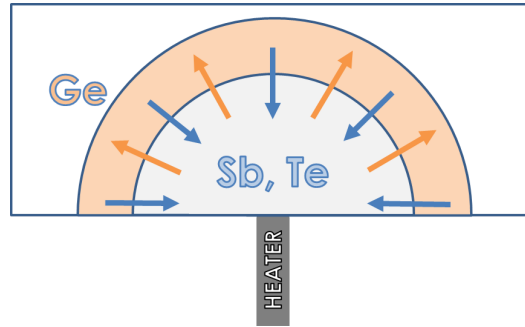


Figure 3.38: Schematic of the atomic migrations observed inside the devices thanks to EELS analyses, showing the depletion of germanium inside the AV, and the concentration of antimony and tellurium.

Nonetheless, it is important to note that all the germanium is not expelled from the AV. In fact, looking at the quantitative analyses performed inside the AV of the cells, we saw that a large amount of Ge still remained in this region. The lowest Ge concentration has been measured inside the AV of the Multi-RESET device to which we applied 10^7 RESET pulses, which is much more than the other devices. The second lowest concentration corresponds to the SETMIN device, which has also undergone a large number of electrical pulses. This means that the composition of the phase change material inside the AV is affected by each pulse applied to the cell. Another observation comes from the results obtained on the GST device, where the same migration behavior is observed: here again germanium has been expelled from the AV, even though the GST phase is known to be very stable. This is the reason why the Ge-rich devices exhibit a better data retention than standard GST devices: germanium (which is the key element to stabilize the phase change material) is partially expelled from the AV in both materials, but the high initial Ge-content of our optimized alloy enables to maintain a Ge-rich composition at the core of the cell, thus improving the thermal stability of the amorphous phase.

3.5 Chapter conclusion

The analyses presented in this chapter helped us to understand the origins of the reliability issues which constitute the main topic of this work. We started by describ-

ing the procedure used to program the devices, and how we prepared them for TEM analyses using the FIB tool, with special precautions taken to avoid electrostatic discharges. Thirteen devices have been programmed in 5 different electrical states, namely RESET, Multi-RESET, standard SET, SETMIN and R-SET, which exhibit different drift behaviors as exposed in chapter 2. The TEM analyses performed on these devices allowed us to establish some links between their electrical properties and their structure. In particular, we observed the formation of larger crystalline grains in the AV of the SETMIN devices with respect to the standard SET devices. The AV of the latter showed signs of an incomplete recrystallization, leading to smaller crystalline grains with remains of amorphous material at their boundaries, thus explaining the higher resistance and drift coefficient values than the SETMIN devices. Concerning the R-SET devices, their low resistance and drift coefficients have been attributed to the creation of a crystalline column inside the AV, crossing the amorphous dome formed during the RESET pulse, and connecting the heater to the top electrode with crystalline grains comparable in size as the ones observed in the SETMIN devices. This peculiar structure enables a good conduction of current in these devices, and lowers the amount of amorphous material on the conduction path, leading to the reduction of the structural relaxations implied in the drift of the resistance.

The EELS measurements also gave us information about the role of elemental migrations on the thermal stability of our Ge-rich devices. Indeed, the EELS maps performed showed the same atomic migrations in all the devices under analyses, with the depletion of germanium inside the AV and the concentration of antimony and tellurium. The germanium enrichment of the alloys enables to keep a higher Ge concentration inside the AV of our cells when compared to standard GST devices. The crystallization temperature of the material in this area is thus still higher than pure GST, hence the improved thermal stability.

At last, the results of the simulations based on the phase-field method gave us important insights into the influence of the SET current on the shape of the crystallized domain. In particular, the peculiar structure observed in the R-SET devices was successfully reproduced, resulting from the growth of the crystalline grain above the AV toward the heater and across the amorphous dome left by the RESET pulse.

General Conclusion

The study of the semiconductor memories market, and the evolution and limits of mainstream memory technologies (i.e. Nand Flash and DRAM) highlighted the need to find new memory technology alternatives able to push further the density increase demands and fulfill the memory hierarchy gap, while maintaining the usual cost decrease. Among the emerging non-volatile memories, the PCM technology present several advantages (scalability, write/erase speed, programming window, multi-level capability) and has reached in the last decade a good level of maturity. This makes it the most promising alternative to Flash devices. In order to answer the restrictive requirements for specific embedded applications (such as Secure Smart-Card and automotive μ controllers), new types of phase-change materials have been developed, with higher content of germanium with respect to standard $\text{Ge}_2\text{Sb}_2\text{Te}_5$. These Ge-rich materials allow for a better retention of the RESET state, but they also lead to the increase of the resistance drift in the SET state, which causes reliability issues. In this Phd, we have shown that by programming the devices with different electrical pulse sequences (with procedures such as the staircase down sequence, or with the less time-consuming R-SET pulse), the drifting behavior of the SET state could be minimized. In parallel, we investigated the physical mechanisms responsible for the drift phenomenon in the SET states and the improvement of data retention in the RESET states, by means of a TEM study of the devices programmed in different resistance states. The results of this study have shown structural differences between the active zones of the devices, which allowed to link the resistance drift to amorphous residues on the conduction path inside the cells. Concerning the improvement of data retention in the RESET state, EELS measurements helped us to understand the atomic migrations taking place inside the devices, showing how Ge-rich materials enabled to keep a higher Ge concentration in the active zone of our devices with respect to standard GST cells. With this knowledge, we can think about new ways to control the drift of the resistance in final products by conceiving special circuits to generate the R-SET pulse. It should be mentioned that further optimization of PCMs is also expected with the development of confined devices integrating Ge-rich materials, which are likely to reduce RESET currents while fulfilling the thermal stability requirements for embedded applications. This would allow the PCM technology to address new markets and take a step forward in its industrialization.

Publications & Conferences

- "Trade-off Between SET and Data Retention Performance Thanks to Innovative Materials for Phase-Change Memory", G. Navarro, **M. Coué**, A. Kioussoglou, P. Noé, F. Fillot, V. Delaye, A. Persico, M. Bernard, C. Sabbione, D. Blachier, V. Sousa, L. Perniola, S. Maitrejean, A. Cabrini, G. Torelli, P. Zuliani, R. Annunziata, E. Palumbo, M. Borghi, G. Reimbold, B. De Salvo, **IEDM 2013**
- "TEM study of low resistance states in Phase Change Memories", **M. Coué**, G. Navarro, V. Sousa, V. Delaye, L. Perniola, N. Bernier, P. Noé, F. Fillot, C. Sabbione, D. Blachier, P. Zuliani, R. Annunziata, G. Reimbold, **MRS 2014**
- "TEM study of low resistance states in Phase Change Memories", **M. Coué**, G. Navarro, V. Sousa, V. Delaye, L. Perniola, N. Bernier, P. Noé, F. Fillot, C. Sabbione, D. Blachier, P. Zuliani, R. Annunziata, G. Reimbold, **CIMTEC 2014**
- "SET Performance Improvement in Phase-Change Memory Based on Innovative Materials Featuring High Temperature Data Retention", G. Navarro, **M. Coué**, A. Kioussoglou, P. Noé, F. Fillot, V. Delaye, A. Persico, A. Roule, M. Bernard, C. Sabbione, D. Blachier, V. Sousa, L. Perniola, S. Maitrejean, A. Cabrini*, G. Torelli, P. Zuliani, R. Annunziata, E. Palumbo, M. Borghi, G. Reimbold, B. De Salvo, **ePCOS 2014**
- "Understanding the High Temperature Data Retention performances of 12Mb Phase Change Memory with optimized Ge-rich GST", V. Sousa, G. Navarro, N. Castellani, **M. Coué**, O. Cueto, C. Sabbione, P. Noé, L. Perniola, S. Blonkowski, P. Zuliani, R. Annunziata, **VLSI 2015**
- "Analysis of SET and RESET states drift of Phase-Change Memories by Low Frequency Noise measurements", S. Souiki, V. Sousa, G. Ghibaudo, G. Navarro, **M. Coué**, L. Perniola, P. Zuliani, R. Annunziata, **IRPS 2015**
- "Crystallization Mechanisms of Low Resistance States in Ge-rich GST Phase-Change Memories", **M. Coué**, V. Sousa, G. Navarro, V. Delaye, N. Bernier, O. Cueto, C. Sabbione, L. Perniola, B. De Salvo, P. Zuliani, R. Annunziata, **ePCOS 2015**

Deposition of the Phase-Change Material

The phase-change materials studied in this thesis have been deposited using the Physical Vapor Deposition (PVD) technique at room temperature. During this type of deposition, the surface of the substrate is covered by atoms sputtered from one or several targets. The sputtering of the targets is achieved thanks to the creation of a plasma inside the chamber, which is done by applying a voltage bias between the cathode (target) and the anode (substrate), thus exciting the atoms of the gas introduced inside the chamber. This gas is generally made of a neutral gas (like argon) and a reactive gas (like nitrogen or propene). The plasma thus made of electrons, which move toward the anode, and cations, which move toward the target. These cations are accelerated by the electrical field, and cause the sputtering of the target atoms when they collide them (fig.A.1).

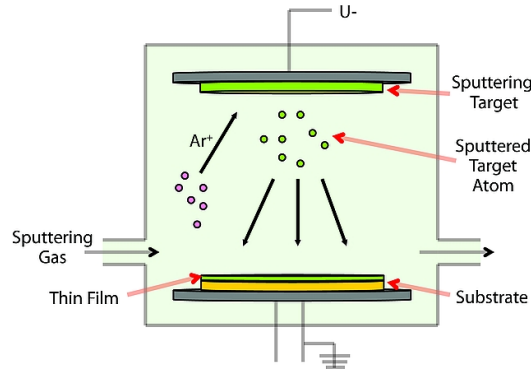


Figure A.1: Schematic of PVD working principle.

However, the slow ionization rate of the gas inside the chamber limits the speed of the deposition. Therefore, the deposition of the phase-change material are accelerated by using the magnetron effect. Thanks to a magnetic field applied to the gas, electrons trajectories are improved in the vicinity of the cathode, thus increasing the ionization probabilities. More ions are then created, leading to higher number of sputtered atoms from the target, and a faster deposition speed.

The materials studied in this thesis have all been deposited using magnetron sputtering. The machines used for this step have three deposition chambers and one surface preparation chamber (fig.A.2). If it is necessary, the surface preparation chamber is used to clean the surface of the layer onto which the material is going to

be deposited. The deposition of the phase-change material is then achieved in the co-sputtering chamber which can present up to three different targets for simultaneous deposition. By tuning the power applied to each target, it is possible to control the amount of materials which is deposited, and thus the composition of the final phase-change material.

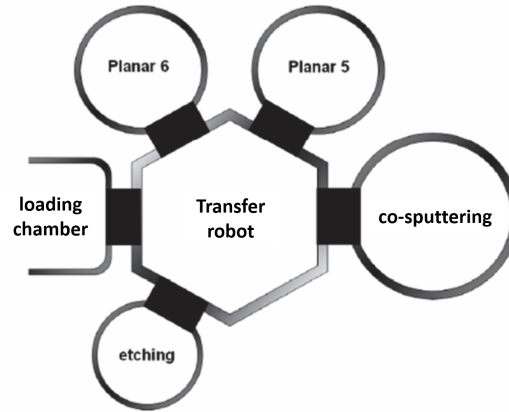


Figure A.2: Schematic of the PVD machines used for the deposition of the phase-change materials.

The FIB instrument

Focused ion beam, also known as FIB, is a technique used particularly in the semiconductor industry, materials science and increasingly in the biological field for site-specific analysis, deposition, and ablation of materials. A FIB setup is a scientific instrument that resembles a scanning electron microscope (SEM). However, while the SEM uses a focused beam of electrons to image the sample in the chamber, a FIB setup uses a focused beam of ions instead. FIB can also be incorporated in a system with both electron and ion beam columns, allowing the same feature to be investigated using either of the beams.

B.1 Principle

FIB systems operate in a similar manner to a scanning electron microscope (SEM) except that a finely focused beam of ions that can be operated at low currents for imaging or high currents for site specific sputtering or milling [Ullaut 1997]. As depicted in fig.B.1, the gallium (Ga^+) primary ion beam hits the sample surface and sputters a small amount of material, which leaves the surface as either secondary ions (i^+ or i^-) or neutral atoms (n^0). The primary beam also produces secondary electrons (e^-). As the primary beam rasters on the sample surface, the signal from the sputtered ions or secondary electrons is collected to form an image.

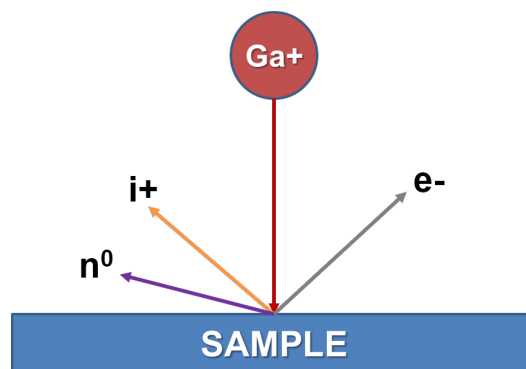


Figure B.1: Principle of FIB ablation using gallium ions. The interaction between the sample and the Ga ions results in the emission of secondary ions (i^+ or i^-), neutral atoms (n^0) and secondary electrons (e^-).

At low beam currents, very little material is sputtered and modern FIB systems can easily achieve 5 nm imaging resolution (imaging resolution with Ga ions is

limited to ≈ 5 nm by sputtering and detector efficiency). At higher primary currents, a great deal of material can be removed by sputtering, allowing precision milling of the specimen down to a sub micrometer or even a nano scale. In order to protect the devices buried in the bulk of the sample, it is common to deposit a layer of a few microns of metallic material such as tungsten before ablation. This deposition, called ion beam induced deposition, is made possible thanks to the injection of a gas (in our case tungsten carboxyl $W(CO)_6$) into the vacuum chamber. By scanning an area with the beam, the precursor gas will be decomposed into volatile and non-volatile components; the non-volatile component remains on the surface as a deposition. Tungsten metal deposition also allows metal lines to be put right where needed, which can be very useful to avoid electrostatic discharges as demonstrated in chapter 3 of this thesis.

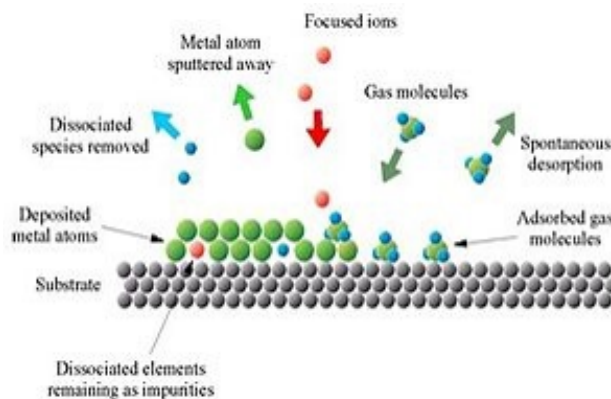


Figure B.2: Principle of gas-assisted deposition in the FIB.

B.2 The instrument

Fig.B.3 shows a schematic of a FIB column, which can be divided into 3 main parts:

- the upper part which generates the beam comprises an ion source (see next section), a suppressor and an extractor;
- then the beam goes through several apertures and lenses in order to control the amount of current arriving on the sample;
- the last part enables the scanning of the sample, as in a SEM, and control the resolution of the etching.

The instrument used for the preparation of the samples presented in this work, a FEI strata 400, is illustrated in fig.B.3. The FIB column can be seen, next to the FEG electron column. The tungsten gas injector allows the deposition of tungsten on the sample, while the Omniprobe is used to take the chunk out of the sample after ablation and to fix it on the copper grid dedicated to TEM observations.

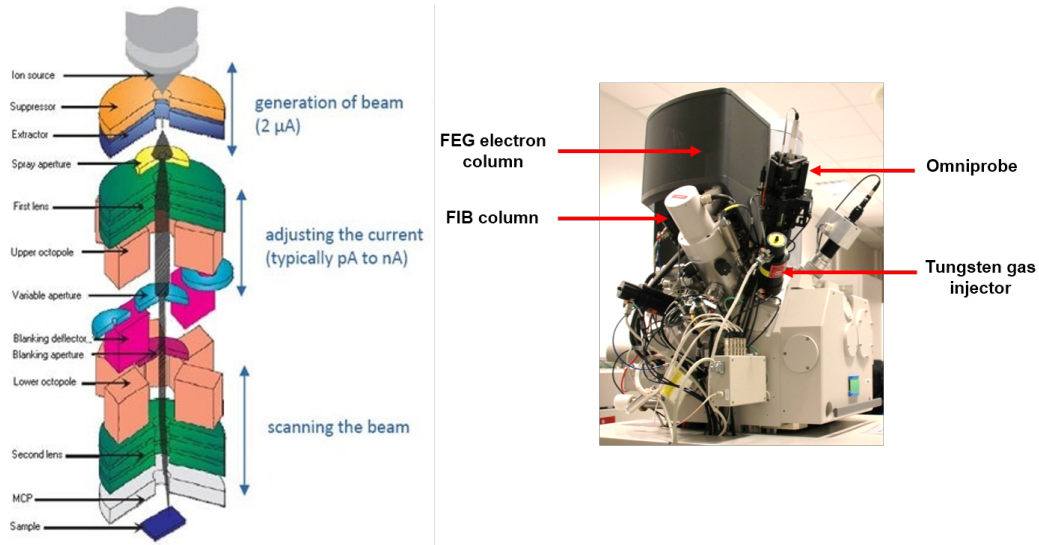


Figure B.3: Schematic of the FIB column (left), and picture of the FEI strata 400 used for the preparation of the TEM samples (right).

B.3 Ion Beam Source

The FEI strata 400 relies on a gallium source which provides the Ga ions for the etching of the samples. In such a source, gallium metal is placed in contact with a tungsten needle. The heated gallium wets the tungsten and flows to the tip of the needle where the opposing forces of surface tension and electric field form the gallium into a cusp shaped tip called a Taylor cone. The tip radius of this cone is extremely small (≈ 2 nm) and results in the creation of a huge electric field (greater than 10^8 volts per centimeter) which causes the ionization and field emission of the gallium atoms. The Ga ions are then accelerated to an energy of 1 to 30 keV, and focused onto the sample by electrostatic lenses.

Transmission Electron Microscopy

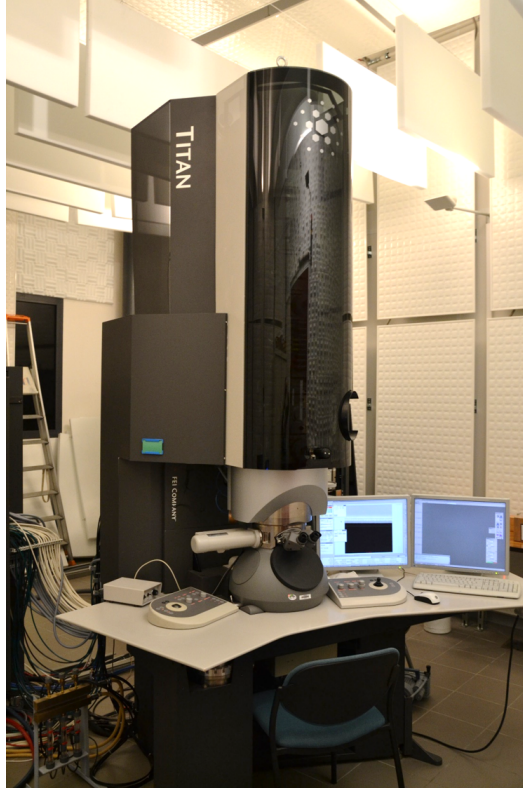


Figure C.1: The FEI Titan microscope, used for the imaging of the samples presented in this work.

Here we present the principles of Transmission Electron Microscopy, with a description of the TEM instruments and the different techniques used for the characterization of the samples presented in this work. The following information was gathered and summed up from [Williams 2009].

C.1 Principle

Following Abbe's theory [Abbe 1873], the maximum resolution achievable with an optical microscope is directly linked to the wavelength of the photons, and to the numerical aperture (NA) of the system. The resolution limit d of a microscope, i.e. the smallest distance below which two neighboring points will no longer be distinguished, is given by:

$$d = \frac{0.61\lambda}{n \sin(\alpha)} = \frac{0.61\lambda}{NA} \quad (\text{C.1})$$

Where λ is the wavelength of the incoming photons, n is the refractive index of the viewing medium, and α is the semi-angle of collection of the magnifying lens. In the early twentieth century, the idea came to push the limit imposed by the relatively long wavelength of visible light (≈ 400 to 800 nanometers), by involving electrons, which we knew from wave mechanics theorized by de Broglie that they had both the properties of particles and waves. This idea suggested that an electron beam could be treated the same way as an electromagnetic wave in order to obtain an image of a sample, hence getting around the limitations of visible light.

The wavelength of electrons is related to their kinetic energy via the de Broglie equation, with an additional correction to account for relativistic effects, as electrons' velocity approaches the speed of light c in a TEM:

$$\lambda_e \approx \frac{h}{\sqrt{2m_0E(1 + \frac{E}{2m_0c^2})}} \quad (\text{C.2})$$

where h is Planck's constant, m_0 is the rest mass of an electron and E is the energy of the accelerated electron. From this equation we see that the wavelength of electrons diminishes as more energy is given to them, thus leading to better resolutions. In an electron microscope, the electrons are generated and accelerated by an electron gun comprising a source and an electric field, which is produced by a potential difference between the source and an anode. The electron beam then interacts with the sample with a spatial contrast due to differences of crystallinity, density or chemical composition.

Typically, a Transmission Electron Microscope provides two main operating modes (fig.C.2):

- Conventional TEM mode, in which the electron beam is kept parallel while arriving on the sample;
- Scanning mode (STEM), in which the electron beam is focused to form a small probe which is scanned over the sample in a raster.

In conventional TEM mode, the electron beam interacts with the sample depending on the thickness, density or chemical composition of the object, thus leading to the formation of a contrasted image by transparency of the observed area. This mode also enables to obtain diffraction patterns, which are based on the wave behavior of electrons: when an electron wave hit a sample with crystalline structures, diffraction happens. The incoming wave is diffracted in multiple secondary waves which are then recombined to form a so-called diffraction pattern. These patterns are very useful to determine the crystalline characteristics of the materials under observation.

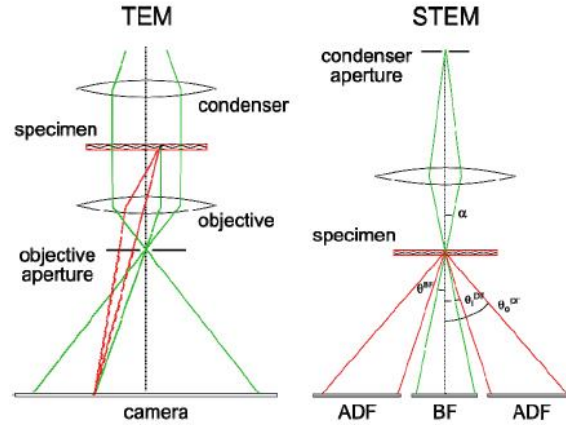


Figure C.2: The two operating modes of a classical Transmission Electron Microscope: conventional TEM (left) and Scanning TEM (right).

In STEM mode, the image is created by collecting the signals emitted from the interaction of the probe (i.e. the focused beam) with the sample on each point of the scanning.

C.2 The TEM instrument

A typical TEM is made of the following main elements (fig.C.3):

- An electron gun, which provides the electron beam;
- Electromagnetic lenses to focus the beam;
- A detector system to form the image.

All these elements are placed in vacuum (from 10^{-7} mbar for the detector to 10^{-10} mbar for the electron gun), which ensure that the electrons will not interact with any foreign particles. A cold trap (made of copper wires linked to a reservoir of liquid nitrogen) is also used to cool down the region near the sample. This system allows to condense the impurities remaining in these zone, keeping them from contaminating the sample.

C.2.1 The electron gun

As said above, the electron beam in a TEM is generated by an electron gun. In our case, the electrons are generated by a tungsten tip under a strong electric field (Field Emission Gun or FEG, fig.C.4), providing highly coherent electrons which ensure a good resolution of the images.

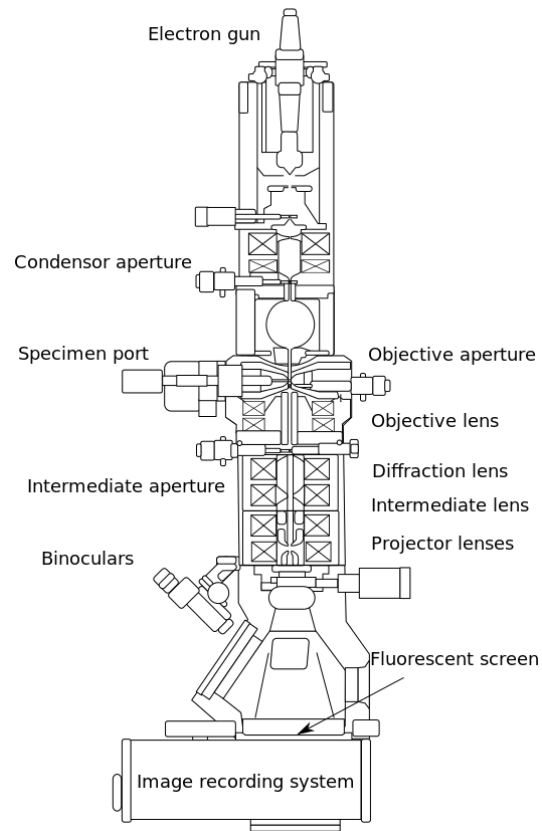


Figure C.3: Schematic of a Transmission Electron Microscope with its main components.

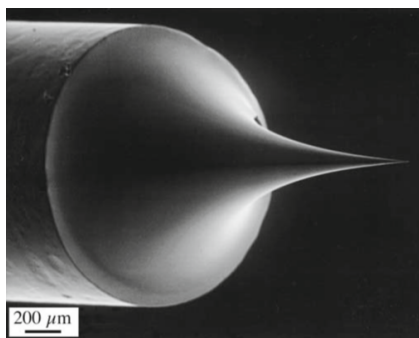


Figure C.4: A FEG tip, showing the fine tungsten needle.

C.2.2 Electromagnetic lenses

Electron lenses are designed to act in a similar manner than an optical lens, by focusing parallel rays at some constant focal length, but using electromagnetic coils instead of glass lenses. The electrons movement in the electromagnetic lenses is thus governed by Lorentz force $\vec{F} = -e\vec{v} \times \vec{B}$. As this force doesn't imply any work, the electrons are deviated without losing any energy when passing through the magnetic field. Fig.C.5 shows a schematic of the inside of an electron lens: the components include the yoke, the magnetic coil, the poles, the polepiece, and the external control circuitry. For these lenses the field produced must be radially symmetric, as deviation from the radial symmetry of the magnetic lens causes aberrations such as astigmatism, and worsens spherical and chromatic aberration.

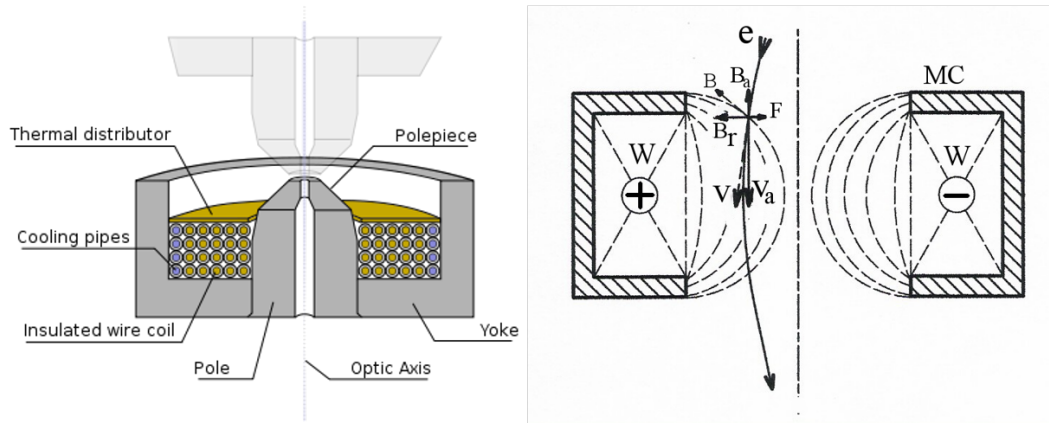


Figure C.5: Cross section view of a typical electromagnetic lens (left) showing its main components. The electrons are deviated because of the Lorentz force applied to them (right).

C.2.3 Apertures

Apertures are annular metallic plates, through which electrons that are further than a fixed distance from the optic axis may be excluded. These consist of a small metallic disc that is sufficiently thick to prevent electrons from passing through the disc, whilst permitting axial electrons. This permission of central electrons in a TEM causes two effects simultaneously: firstly, apertures decrease the beam intensity as electrons are filtered from the beam, which may be desired in the case of beam sensitive samples. Secondly, this filtering removes electrons that are scattered to high angles, which may be due to unwanted processes such as spherical or chromatic aberration, or due to diffraction from interaction within the sample.

Apertures are either a fixed aperture within the column, such as at the condenser lens, or are a movable aperture, which can be inserted or withdrawn from the beam path, or moved in the plane perpendicular to the beam path. Aperture assemblies are mechanical devices which allow for the selection of different aperture sizes, which may be used by the operator to trade off intensity and the filtering effect of the

aperture. Aperture assemblies are often equipped with micrometers to move the aperture, required during optical calibration.

C.2.4 Detectors and display

In conventional TEM mode, the transmitted beam is projected on a simple phosphor screen for direct observations, or on a CCD camera for the acquisition of the image.

In STEM mode, the scattered electrons from the interactions of the probe with the sample are collected on semiconductor detectors as depicted in fig.C.6.

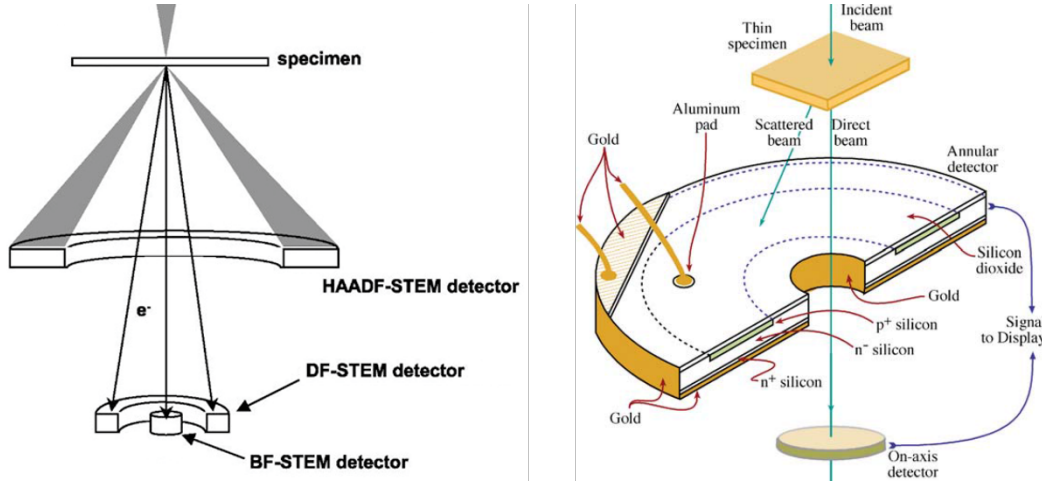


Figure C.6: Schematic of the different detectors used for imaging in STEM mode.

The positions and architectures of the detectors allow to collect either the electrons strongly scattered (Dark Field imaging), or the ones scattered at smaller angles (Bright Field imaging). The image is finally obtained by reconstruction of the signals gathered from all the points scanned.

C.3 Bright Field imaging in conventional TEM mode

Contrast formation in conventional TEM mode depends greatly on the mode of operation. Complex imaging techniques, which utilize the unique ability to change lens strength or to deactivate a lens, allow for many operating modes. These modes may be used to discern information that is of particular interest to the investigator. In the next paragraphs we will focus on the two imaging modes used for the characterization of our samples, namely Bright Field (BF) and Dark Field (DF) imaging.

The most common mode of operation for a TEM is the Bright Field imaging mode. In this mode the contrast formation, when considered classically, is formed directly by occlusion and absorption of electrons in the sample. Thicker regions of the sample, or regions with a higher atomic number will appear dark, whilst regions with no sample in the beam path will appear bright - hence the term *Bright Field*.

The image is in effect assumed to be a simple two dimensional projection of the sample down the optic axis.

C.4 Diffraction Patterns and Dark Field imaging

C.4.1 Diffraction Patterns

Instead of looking at the image formed by the transmitted beam, we can be interested in looking at the diffraction of electrons. Indeed, if the sample under observation exhibits crystalline structures, the electron beam can undergo Bragg scattering which disperses electrons into discrete locations in the back focal plane. By tuning the electromagnetic lenses such that the back focal plane of the lens is placed on the imaging apparatus, a diffraction pattern can be generated (fig.C.7).

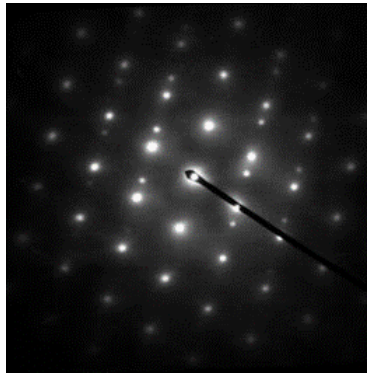


Figure C.7: Crystalline diffraction pattern from a twinned crystalline grain of Austenitic steel.

For thin crystalline samples, this produces an image that consists of a pattern of dots in the case of a single crystal, a series of rings in the case of a polycrystalline material, or blurred disks in the case of amorphous solid material. For the single crystal case the diffraction pattern is dependent upon the orientation of the specimen and the structure of the sample illuminated by the electron beam. This image provides us with information about the space group symmetries in the crystal and the crystal's orientation to the beam path. Practically, the indexation of diffraction patterns (i.e. the identification of the diffraction spots) is done using a dedicated software (JEMS in our case) which emulates the possible patterns for a material of known stoichiometry at various orientations, and compare those to the experimental data in order to find an eventual match. Note that this supposes that we already have an idea of the material stoichiometry before the indexation.

In our case, the majority of the diffraction patterns presented have been obtained using Nano Beam Diffraction (NBD). In this mode, the electron beam is kept parallel but reduced to the smallest diameter achievable (≈ 5 nm). This enables to investigate on the crystallinity of small crystalline structures at very precise locations.

The NBD patterns given in our studies exhibit disks instead of points. Indeed,

to be able to achieve such a small spatial resolution, the beam has to be slightly convergent, and is thus not perfectly parallel. This convergence results in the widening of the spots, as observed in our patterns.

C.4.2 Dark Field imaging

By the placement of an aperture (the objective aperture) in the back focal plane, we can select (or exclude) specific diffraction spots. Thus, only parts of the sample that are causing the electrons to scatter to the selected diffraction spots will end up projected onto the imaging apparatus. The other parts of the sample which diffract electrons to other angles will appear dark, hence the name *Dark Field*. This imaging mode enables to highlight crystalline grains of a particular orientation in our samples, giving therefore important information about the crystallinity of the material.

C.5 Electron Energy Loss Spectroscopy

Electron energy-loss spectrometry (EELS) is the analysis of the energy distribution of electrons that have come through the specimen. These electrons may have lost no energy or may have suffered inelastic (usually electron-electron) collisions. These energy-loss events provide us information about the chemistry and the electronic structure of the specimen atoms. In order to examine the spectrum of electron energies, we use a magnetic-prism spectrometer, which acts in a similar manner as a prism diffracting visible light into rays of different colors: when entering the magnetic prism, the electrons are deviated by the magnetic field with a strength which depends on the energy of the electrons (fig.C.8).

There is only one kind of spectrometer commercially available, manufactured by Gatan, Inc. termed a parallel-collection EELS or PEELS. The magnetic-prism (sometimes called a magnetic-sector) system is mounted on a TEM or STEM after the viewing screen or post-specimen detectors. A CCD camera is placed at the very end of the system to collect the electrons and form the final spectrum.

An example of an EELS spectrum is shown in fig.C.9. The low-loss region contains electronic information from the more weakly bound conduction and valence-band electrons, while the high-loss region contains information from inelastic interactions with the inner or core shells.

In our case, we will focus on the high-loss region since it enables direct elemental identification. Indeed, when an electron beam transfers sufficient energy to a core-shell electron (i.e., one in the inner, more tightly bound K, L, M, etc., shells) to move it outside the attractive field of the nucleus, the atom is said to be ionized. We call the ionization-loss signal in the EELS spectrum an "edge", and these edges are used as the basis for elemental mapping. For each element of the periodic classification correspond one or several edges which can be found in EELS tables. By looking at these tables we can identify the edges corresponding to the elements we are interested in, namely germanium (1217 eV), antimony (527 eV) and tellurium (577

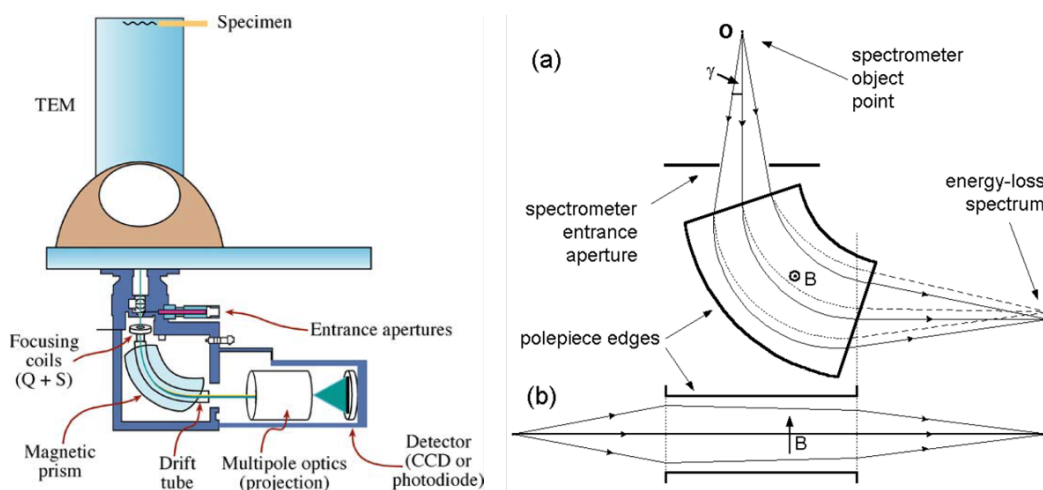


Figure C.8: [LEFT] Schematic diagram showing how a PEELS is interfaced below the viewing screen of a TEM and the position of the various components. [RIGHT] Dispersive and focusing properties of a magnetic prism (a) in a plane perpendicular to the magnetic field and (b) parallel to the field. Solid lines represent zero-loss electrons ($E = 0$); dashed lines represent those that have lost energy during transmission through the specimen.

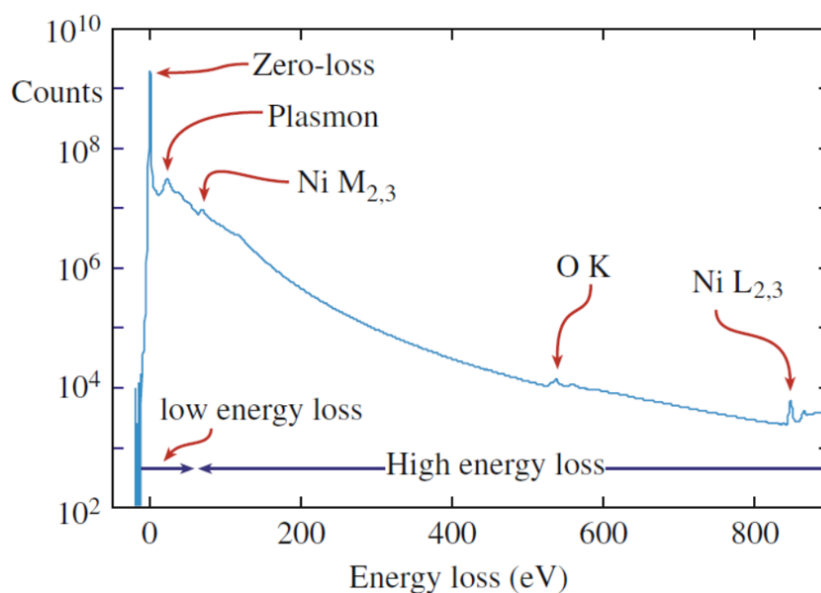


Figure C.9: An EELS spectrum displayed in logarithmic intensity mode. The zero-loss peak is an order of magnitude more intense than the low energy-loss portion, which is many orders of magnitude more intense than the small ionization edges identified in the high energy-loss range. Note the relatively high (and rapidly changing) background.

eV) in our case. From here, we can perform EELS maps as described in chapter 3. The software used for the acquisition of EELS spectra (Digital Micrograph) also allows quantitative analyses. For these analyses, the software determines the number of atoms N responsible for the intensity I of each edge. N is related to I by a sensitivity factor σ , called the partial ionization cross section, which depends on the elements analyzed. The basic equation for quantitative analyses is then given by:

$$I = N \times I_0 \times \sigma \quad (\text{C.3})$$

Where I_0 is the integrated intensity of the zero-loss peak (i.e. the number of electrons which didn't lose any energy). In application, the different edges are integrated on an arbitrary energy range Δ (chosen by the experimenter). The angle of collection β also has to be taken into account for the calculation of the cross section factor. The previous equation then becomes:

$$I(\Delta, \beta) = N \times I_0(\beta) \times \sigma(\Delta, \beta) \quad (\text{C.4})$$

With this equation, we can perform relative quantitative measurements between different elements. For example, in the case of two elements A & B, we have:

$$\frac{N_A}{N_B} = \frac{I_A(\Delta, \beta) \times \sigma_B(\Delta, \beta)}{I_B(\Delta, \beta) \times \sigma_A(\Delta, \beta)} \quad (\text{C.5})$$

The most delicate part of this method is the calculation of the cross sections factors. Indeed, these factors depend on many parameters, such as the incident energy, the convergence angle... Simple models can be used to compute them, as the hydrogenic model, but they are not very accurate. For best results, we used the Hartree-Slater models, which are much more complicated to calculate as based on quantum mechanical equations. These calculations are automatically performed by the Digital Micrograph software, which provides both hydrogenic and Hartree-Slater models.

The simulation tool

D.1 The Level Set Method

The Level Set Method (LSM) enables to simulate the evolution of complex interfaces, as it is the case in phase-change memories where the amorphous/crystalline interface evolves during the pulse application [Gliere 2011]. There are several advantages of using this method:

- intrinsic ability to deal with multiple connected interfaces and their topological changes;
- natural extension to three-dimensional problems;
- capability to provide accurate values of the interface normal and curvature

In the LSM, the interface Γ between two domains is captured as the zero level set of a smooth function ϕ :

$$\Gamma(t) = (x, t) | \phi(x, t) = 0 \quad (\text{D.1})$$

The transient motion of Γ is computed by advecting the level set function ϕ with a velocity field v , defined by the physical problem to solve:

$$\partial\phi/\partial t + v \cdot \text{grad}\phi = 0 \quad (\text{D.2})$$

In our case, Γ lies between the crystal and amorphous phases, and the interface velocity is taken as the crystal growth speed. The chosen level set method is defined as a signed distance, positive in the crystalline phase and negative in the amorphous phase.

D.2 Simulation of nucleation and growth

The equations used for the modeling of crystal nucleation and growth have been introduced in the first chapter, when we presented the physics of crystallization in phase-change materials. They are given back hereafter as a reminder.

D.2.1 Nucleation

The nucleation rate is given by:

$$I = I_s \exp(-\tau/\delta t) \quad (\text{D.3})$$

In which τ is the time needed to establish the stationary state population of nuclei and δt is the isothermal holding time, based on the local temperature variation rate $\delta T/\delta t$. The stationary nucleation rate I_s is defined by:

$$I_s = N \times \gamma \times O_n \times Z_e \times \exp(-\frac{\Delta G^*}{k_B T}) \quad (\text{D.4})$$

Where N is the density of nucleation sites, γ is the atomic jump frequency, Z_e is the Zeldovich factor, O_n^* is the number of atoms at the surface of the critical size nucleus and ΔG^* is the free energy associated to the creation of a stable nucleus.

D.2.2 Growth

The growth speed of a crystalline nucleus (in $m.s^{-1}$) is given by:

$$v(T) = d \times \nu \times (\exp(-\frac{Q}{kT}) - \exp(-\frac{Q + \Delta G_v d^3}{kT})) \quad (\text{D.5})$$

In which ν is the atomic vibration frequency (in s^{-1}), Q is the energy barrier of the liquid to crystal transition (in J), and d is the interatomic distance.

D.3 Coupling the Level Set Method with an electro-thermal solver

The electro-thermal solver used to determine the distributions of electric potential V , electric current density j , and temperature T , relies on the coupled system of partial differential equations formed by the current conservation and heat transfer equations:

$$\text{div}(-\sigma \text{grad} V) = 0 \quad (\text{D.6})$$

$$\rho C_p \partial T / \partial t - \text{div}(-k \text{grad} T) = j^2 / \sigma \quad (\text{D.7})$$

where σ , ρ , C_p and k are respectively the material electrical conductivity, density, heat capacity and thermal conductivity.

The simulation of the threshold switching mechanism is based on the electric field dependence of the amorphous PCM conductivity [Wright 2006]. The conductivities of the crystalline and amorphous phases are also temperature dependent. They are given by:

$$\sigma_{cr} = \sigma_{cr}^0 \exp(-E_{cr}/(kT)) \quad (\text{D.8})$$

$$\sigma_{am} = \sigma_{am}^0 \exp(-E_{am}/(kT)) \exp(E/E_0) \quad (\text{D.9})$$

where σ_{cr}^0 and σ_{am}^0 are prefactors for the conductivities of crystalline and amorphous phases, E_{cr} and E_{am} are the thermal activation energies and E_0 is the critical electric field for switching.

D.4 Numerical methods and implementation

The 2D spatial discretization of the conservation and heat transfer equations is done using the Finite Volume Method which creates an adaptative quadtree grid. The computation of the model presented above includes the following steps:

- calculation of local homogeneous and heterogeneous nucleation rates and crystal growth speed;
- random nucleation in the amorphous material;
- transient evolution of the level set function;
- segmentation of the PCM domain in three different phases (crystalline, amorphous and liquid)

The level set function is computed on a regular mesh, built on the PCM domain only. The stochastic character of nucleation is reproduced as follows: in each LSM mesh cell of the PCM domain, if the temperature is below the melting temperature and the cell is not in the crystalline phase, a Monte Carlo approach of nucleation is used, where the nucleation probability is defined from the local nucleation rates.

Bibliography

- [Abbe 1873] E. Abbe. *Beitrage zur Theorie des Mikroskops und der mikroskopischen Wahrnehmung*. Archiv fur mikroskopische Anatomie, vol. 9, no. 1, pages 413–418, 1873. (Cited on page [101](#).)
- [Ahn 2005] S.J. Ahn, Y.N. Hwang, Y.J. Song, S.H. Lee, S.Y. Lee, J.H. Park, C.W. Jeong, K.C. Ryoo, J.M. Shin, Y. Fai, J.H. Oh, G.H. Koh, G.T. Jeong, S.H. Joo, S.H. Choi, Y.H. Son, J.C. Shin, Kinam Kim, H.S. Jeong and Kinam Kim. *Highly reliable 50nm contact cell technology for 256Mb PRAM*. In VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on, pages 98–99, June 2005. (Cited on page [23](#).)
- [Al Ghamdi 2011] A.A. Al Ghamdi, M.A. Alvi and Shamshad A. Khan. *Non-isothermal crystallization kinetic study on Ga₁₅Se_{85-x}Ag_x chalcogenide glasses by using differential scanning calorimetry*. Journal of Alloys and Compounds, vol. 509, no. 5, pages 2087–2093, 2011. (Cited on page [42](#).)
- [Arreghini 2013] A. Arreghini, G. Van den bosch and J. Van Houdt. *Innovative schemes to improve reliability and density of horizontal and vertical channel 3D Flash*. In Memory Workshop (IMW), 2013 5th IEEE International, pages 151–154, May 2013. (Cited on page [11](#).)
- [Baker 2012] K. Baker. *Embedded Nonvolatile Memories: A Key Enabler for Distributed Intelligence*. In Memory Workshop (IMW), 2012 4th IEEE International, pages 1–4, May 2012. (Cited on pages [8](#) and [9](#).)
- [Bedeschi 2009] F. Bedeschi, R. Fackenthal, C. Resta, E.M. Donze, M. Jagasivamani, E.C. Buda, F. Pellizzer, D.W. Chow, A. Cabrini, G. Calvi, R. Faravelli, A. Fantini, G. Torelli, D. Mills, R. Gastaldi and G. Casagrande. *A Bipolar-Selected Phase Change Memory Featuring Multi-Level Cell Storage*. Solid-State Circuits, IEEE Journal of, vol. 44, no. 1, pages 217–227, Jan 2009. (Cited on page [23](#).)
- [Boniardi 2010] M. Boniardi, D. Ielmini, S. Lavizzari, A.L. Lacaita, A. Redaelli and A. Pirovano. *Statistics of Resistance Drift Due to Structural Relaxation in Phase-Change Memory Arrays*. Electron Devices, IEEE Transactions on, vol. 57, no. 10, pages 2690–2696, Oct 2010. (Cited on page [36](#).)
- [Burr 2013] Burr. *Towards storage class memory: 3-D crosspoint access device using mixed-ionic-electronic-conduction*, 2013. IBM J. Research and Development. (Cited on page [7](#).)
- [Caravati 2011] S Caravati, D Colleoni, R Mazzarello, T D K \tilde{A} $\frac{1}{4}$ hne, M Krack, M Bernasconi and M Parrinello. *First-principles study of nitrogen doping*

- in cubic and amorphous Ge₂Sb₂Te₅*. Journal of Physics: Condensed Matter, vol. 23, no. 26, page 265801, 2011. (Cited on page 44.)
- [Chen 2006] Y.C. Chen, C.T. Rettner, S. Raoux, G.W. Burr, S.-H. Chen, R.M. Shelby, M. Salinga, W.P. Risk, T.D. Happ, G.M. McClelland, M. Breitwisch, A. Schrott, J.B. Philipp, M.H. Lee, R. Cheek, T. Nirschl, M. Lamorey, C.F. Chen, E. Joseph, S. Zaidi, B. Yee, H.L. Lung, R. Bergmann and C. Lam. *Ultra-Thin Phase-Change Bridge Memory Device Using GeSb*. In Electron Devices Meeting, 2006. IEDM '06. International, pages 1–4, Dec 2006. (Cited on page 26.)
- [Chen 2008] Y.C. Chen. *The Bridge Structure for Advanced Phase Change Memory Investigations*. In ePCOS, 2008. (Cited on page 26.)
- [Choi 2010] B.J. Choi. *Switching power reduction in phase change memory cell using CVD Ge₂Sb₂Te₅ and ultrathin TiO₂ films*. J. Electrochemical Society, vol. 156, Jan 2010. (Cited on page 24.)
- [Choi 2014] Jungdal Choi and Kwang Soo Seol. *3D approaches for non-volatile memory*. In VLSI Technology (VLSIT), 2011 Symposium on, pages 178–179, June 2014. (Cited on page 7.)
- [Chung 2011] Hoeju Chung, Byung Hoon Jeong, ByungJun Min, Youngdon Choi, Beak-Hyung Cho, Junho Shin, Jinyoung Kim, Jung Sunwoo, Joon min Park, Qi Wang, Yong-Jun Lee, Sooho Cha, DukMin Kwon, Sangtae Kim, Sunghoon Kim, Yoohwan Rho, Mu-Hui Park, Jaewhan Kim, Ickhyun Song, Sunghyun Jun, Jaewook Lee, KiSeung Kim, Ki won Lim, Won ryul Chung, ChangHan Choi, HoGeun Cho, Inchul Shin, Woochul Jun, Seokwon Hwang, Ki-Whan Song, Kwangjin Lee, Sang whan Chang, Woo-Yeong Cho, Jei-Hwan Yoo and Young-Hyun Jun. *A 58nm 1.8V 1Gb PRAM with 6.4MB/s program BW*. In Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International, pages 500–502, Feb 2011. (Cited on page 17.)
- [Czubatyj 2010] W. Czubatyj. *Nanocomposite Phase-Change Memory Alloys for Very High Temperature Data Retention*. IEEE, vol. 31, no. 8, pages 869–871, 2010. (Cited on pages 56 and 58.)
- [De Charentenay 2015] De Charentenay. *Emerging Non volatile Memory (NVM) Market Trends - Technological choices are about to be made by key players*, 2015. Leti Memory Workshop. (Cited on pages 3 and 7.)
- [de la Pena 2015] Francisco de la Pena, Pierre Burdet, Tomas Ostasevicius, Mike Sarahan, Magnus Nord, Vidar Tonaas Fauske Josh Taillon, Alberto Eljarrat, Stefano Mazzucco, Gael Donval, Luiz Fernando Zagonel, Michael Walls and Ilya Iyengar. *hyperspy: HyperSpy 0.8.1*, August 2015. (Cited on page 69.)

- [Dewald 1966] J.F. Dewald, W.R. Northover and A.D. Pearson. *Multiple resistance semiconductor elements*, March 15 1966. US Patent 3,241,009. (Cited on page 15.)
- [Du 2015] P.Y. Du. *The impact of melting during reset operation on the reliability of phase change memory*. In IEEE 2012, 2015. (Cited on page 61.)
- [EETimes 2006] EETimes. *Samsung introduces working prototype of PRAM*, 2006. "<http://www.eetimes.com/>". (Cited on page 17.)
- [Friedrich 2000] I. Friedrich, V. Weidenhof, W. Njoroge, P. Franz and M. Wuttig. *Structural transformations of Ge₂Sb₂Te₅ films studied by electrical resistance measurements*. Journal of Applied Physics, vol. 87, no. 9, pages 4130–4134, 2000. (Cited on page 42.)
- [Gliere 2011] A. Gliere, O. Cueto and J. Hazart. *Coupling the level set method with an electrothermal solver to simulate GST based PCM cells*. In Simulation of Semiconductor Processes and Devices (SISPAD), 2011 International Conference on, pages 63–66, Sept 2011. (Cited on pages 31, 84 and 111.)
- [Greene 2008] Kate Greene. *Technology Review*, 2008. "<http://www.technologyreview.com/news/409482/a-memory-breakthrough/>". (Cited on page 17.)
- [Gyanathan 2012] A. Gyanathan and Y.C. Yeo. *Two-bit multi-level phase change random access memory with a triple phase change material stack structure*. In J. Appl. Phys., 2012. (Cited on page 23.)
- [Hitachi 2005] Hitachi and Renesas. *Hitachi and Renesas Technology Develop Low-Power MOS Phase-Change Memory Cells for On-Chip Memory of Microcontrollers*, 2005. "<http://www.hitachi.com/New/cnews/051213.html>". (Cited on page 17.)
- [Hubert 2011] Q. Hubert, C. Jahan, A. Toffoli, L. Perniola, V. Sousa, A. Persico, J.-F. Nodin, H. Grampeix, F. Aussenac and B. De Salvo. *Reset current reduction in phase-change memory cell using a thin interfacial oxide layer*. In Solid-State Device Research Conference (ESSDERC), 2011 Proceedings of the European, pages 95–98, September 2011. (Cited on page 23.)
- [Hubert 2013] Quentin Hubert. *Optimisation de memoires PCRAM pour generations sub-40 nm : integration de matériaux alternatifs et structures innovantes*. PhD thesis, University of Grenoble, 2013. (Cited on page 19.)
- [Hyot 2002] B Hyot, L Poupinet, V Gehanno and P.J Desre. *Analysis of writing and erasing behaviours in phase change materials*. Journal of Magnetism and Magnetic Materials, vol. 249, no. 3, pages 504 – 508, 2002. Proceedings of the First European Workshop on Innovative Mass Storage Technologies, IMST01. (Cited on page 30.)

- [Ielmini 2007a] D. Ielmini, A.L. Lacaita and D. Mantegazza. *Recovery and Drift Dynamics of Resistance and Threshold Voltages in Phase-Change Memories*. Electron Devices, IEEE Transactions on, vol. 54, no. 2, pages 308–315, Feb 2007. (Cited on pages 20 and 53.)
- [Ielmini 2007b] D. Ielmini, S. Lavizzari, D. Sharma and A.L. Lacaita. *Physical interpretation, modeling and impact on phase change memory (PCM) reliability of resistance drift due to chalcogenide structural relaxation*. In Electron Devices Meeting, 2007. IEDM 2007. IEEE International, pages 939–942, Dec 2007. (Cited on page 36.)
- [ITRS 2012] ITRS. *Emerging Research Devices*, 2012. International Technology Roadmap for Semiconductors. (Cited on page 22.)
- [Jang 2009] Jaehoon Jang, Han-Soo Kim, Wonseok Cho, Hoosung Cho, Jinho Kim, Sun Il Shim, Younggoan Jang, Jae-Hun Jeong, Byoung-Keun Son, Dong Woo Kim, Kihyun, Jae-Joo Shim, Jin Soo Lim, Kyoung-Hoon Kim, Su Youn Yi, Ju-Young Lim, Dewill Chung, Hui-Chang Moon, Sungmin Hwang, Jong-Wook Lee, Yong-Hoon Son, U-in Chung and Won-Seong Lee. *Vertical cell array using TCAT(Terabit Cell Array Transistor) technology for ultra high density NAND flash memory*. In VLSI Technology, 2009 Symposium on, pages 192–193, June 2009. (Cited on page 10.)
- [JEMS 2015] JEMS. *Diffraction patterns indexation using JEMS software*, 2015. "<http://cime.epfl.ch/research/jems>". (Cited on page 71.)
- [Jung 2006] Soon-Moon Jung, Jaehoon Jang, Wonseok Cho, Hoosung Cho, Jaehun Jeong, Youngchul Chang, Jonghyuk Kim, Youngseop Rah, Yangsoo Son, Junbeom Park, Min-Sung Song, Kyoung-Hon Kim, Jin-Soo Lim and Kinam Kim. *Three Dimensionally Stacked NAND Flash Memory Technology Using Stacking Single Crystal Si Layers on ILD and TANOS Structure for Beyond 30nm Node*. In Electron Devices Meeting, 2006. IEDM '06. International, pages 1–4, Dec 2006. (Cited on page 10.)
- [Kaban 2004] I. Kaban, E. Dost and W. Hoyer. *Thermodynamic and structural investigations of heat-treated amorphous Ge-Te alloys*. Journal of Alloys and Compounds, vol. 379, no. 1-2, pages 166–170, 2004. (Cited on page 42.)
- [Kim 2005] Kinam Kim and Su Jin Ahn. *Reliability investigations for manufacturable high density PRAM*. In Reliability Physics Symposium, 2005. Proceedings. 43rd Annual. 2005 IEEE International, pages 157–162, April 2005. (Cited on page 24.)
- [Kim 2009] Jiyoung Kim, A.J. Hong, Sung Min Kim, Emil B. Song, Jeung Hun Park, Jeonghee Han, Siyoung Choi, Deahyun Jang, Joo Tae Moon and K.L. Wang. *Novel Vertical-Stacked-Array-Transistor (VSAT) for ultra-high-density and cost-effective NAND Flash memory devices and SSD (Solid State*

- Drive*). In VLSI Technology, 2009 Symposium on, pages 186–187, June 2009. (Cited on page 10.)
- [Kim 2011] SangBum Kim. *Resistance and Threshold Switching Voltage Drift Behavior in phase-change memory and Their Temperature Dependence at Microsecond Time Scales Studied Using a Micro-Thermal Stage*. Electron Devices, IEEE Transactions on, vol. 58, no. 3, pages 584–592, 2011. (Cited on page 36.)
- [Kissinger 1957] H. E. Kissinger. *Reaction Kinetics in Differential Thermal Analysis*. Analytical Chemistry, vol. 29, no. 11, pages 1702–1706, 1957. (Cited on page 42.)
- [Kostylev 2008] S. Kostylev. *Drift of programmed resistance in electrical phase change memory devices*. In EPCOS 2008, 2008. (Cited on page 85.)
- [Krishnamurthy 2011] R. Krishnamurthy. *Inside the Samsung 512 Mb Phase Change Memory*, 2011. "<http://ww3.chipworks.com/ko/technical-competitive-analysis/resources/blog/a-peek-inside-the-samsung-512-mb-4f2-cross-point-phase-change-memory/>". (Cited on page 17.)
- [Krishnamurthy 2012] R. Krishnamurthy. *First Volume Production Phase Change Memory by Micron*, 2012. "<http://ww3.chipworks.com/ja/technical-competitive-analysis/resources/blog/first-volume-production-phase-change-memory-by-micron/>". (Cited on page 17.)
- [Lacaita 2007] A.L. Lacaita and D. Ielmini. *Reliability issues and scaling projections for phase change non volatile memories*. In Electron Devices Meeting, 2007. IEDM 2007. IEEE International, pages 157–160, Dec 2007. (Cited on pages 34 and 35.)
- [Lai 2001] S. Lai and T. Lowrey. *OUM - A 180 nm nonvolatile memory cell element technology for stand alone and embedded applications*. In Electron Devices Meeting, 2001. IEDM '01. Technical Digest. International, pages 36.5.1–36.5.4, Dec 2001. (Cited on page 49.)
- [Lai 2003] S. Lai. *Current status of the phase change memory and its future*. In Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International, pages 10.1.1–10.1.4, Dec 2003. (Cited on page 22.)
- [Lee 2007] J.I. Lee, H. Park, S.L. Cho, Y.L. Park, B.J. Bae, J.H. Park, J.S. Park, H.G. An, J.S. Bae, D.H. Ahn, Y.T. Kim, H. Horii, S.A. Song, J.C. Shin, S.O. Park, H.S. Kim, U-in Chung, J.T. Moon and B.-I. Ryu. *Highly Scalable Phase Change Memory with CVD GeSbTe for Sub 50nm Generation*. In VLSI Technology, 2007 IEEE Symposium on, pages 102–103, June 2007. (Cited on page 26.)

- [Lue 2010] Hang-Ting Lue, Tzu-Hsuan Hsu, Yi-Hsuan Hsiao, S.P. Hong, M.T. Wu, F.H. Hsu, N.Z. Lien, Szu-Yu Wang, Jung-Yu Hsieh, Ling-Wu Yang, Tahone Yang, Kuang-Chao Chen, Kuang-Yeu Hsieh and Chih-Yuan Lu. *A highly scalable 8-layer 3D vertical-gate (VG) TFT NAND Flash using junction-free buried channel BE-SONOS device*. In VLSI Technology (VLSIT), 2010 Symposium on, pages 131–132, June 2010. (Cited on page 10.)
- [Matsui 2006] Y. Matsui. *Ta₂O₅ interfacial layer between GST and W plug enabling low power operation of phase change memories*. In IEDM, 2006. (Cited on page 24.)
- [Natarajan 2009] S. Natarajan, S. Chung, L. Paris and A. Keshavarzi. *Searching for the dream embedded memory*. Solid-State Circuits Magazine, IEEE, vol. 1, no. 3, pages 34–44, Summer 2009. (Cited on page 5.)
- [Navarro 2013] Gabriele Navarro. *Trade-off Between SET and Data Retention Performances Thanks to Innovative Materials for Phase-Change Memory*. IEDM 2013, 2013. (Cited on page 37.)
- [Niebel 2011] A. Niebel. *Embedded Non Volatile Memory Markets on the Rise*. In Memory Workshop (IMW), 2011 3rd IEEE International, pages 15–17, 2011. (Cited on page 8.)
- [Nirschl 2007] T. Nirschl, J.B. Philipp, T.D. Happ, G.W. Burr, B. Rajendran, M.H. Lee, A. Schrott, M. Yang, M. Breitwisch, C.F. Chen, E. Joseph, M. Lamorey, R. Cheek, S.-H. Chen, S. Zaidi, S. Raoux, Y.C. Chen, Y. Zhu, R. Bergmann, H.L. Lung and C. Lam. *Write Strategies for 2 and 4-bit Multi-Level Phase-Change Memory*. In Electron Devices Meeting, 2007. IEDM 2007. IEEE International, pages 461–464, Dec 2007. (Cited on page 23.)
- [Numonyx 2009] Numonyx. *Numonyx to Present Phase Change Memory Research Results at Leading Technology Industry Conference*, 2009. "<http://investors.micron.com/releasedetail.cfm?ReleaseID=467227>". (Cited on page 17.)
- [Oh 2009] G.H. Oh, Y.L. Park, J.I. Lee, D.H. Im, J.S. Bae, D.H. Kim, D.H. Ahn, H. Horii, S.O. Park, H.S. Yoon, I.S. Park, Y.S. Ko, U-in Chung and J.T. Moon. *Parallel multi-confined (PMC) cell technology for high density MLC PRAM*. In VLSI Technology, 2009 Symposium on, pages 220–221, June 2009. (Cited on page 23.)
- [Ottogalli 2004] F. Ottogalli, A. Pirovano, F. Pellizzer, M. Tosi, P. Zuliani, P. Bone-talli and R. Bez. *Phase-change memory technology for embedded applications*. In Solid-State Device Research conference, 2004. ESSDERC 2004. Proceeding of the 34th European, pages 293–296, Sept 2004. (Cited on page 22.)

- [Ovshinsky 1968] Stanford R. Ovshinsky. *Reversible Electrical Switching Phenomena in Disordered Structures*. Phys. Rev. Lett., vol. 21, pages 1450–1453, Nov 1968. (Cited on page 15.)
- [Padilla 2011] Alvaro Padilla, Geoffrey W. Burr, Charles T. Rettner, Teya Topuria, Philip M. Rice, Bryan Jackson, Kumar Virwani, Andrew J. Kellock, Diego Dupouy, Anthony DeBunne, Robert M. Shelby, Kailash Gopalakrishnan, Rohit S. Shenoy and B. N. Kurdi. *Voltage polarity effects in Ge₂Sb₂Te₅-based phase change memory devices*. Journal of Applied Physics, vol. 110, no. 5, 2011. (Cited on pages 49 and 54.)
- [Pellizzer 2004] F. Pellizzer, A. Pirovano, F. Ottogalli, M. Magistretti, M. Scavaggi, P. Zuliani, M. Tosi, A. Benvenuti, P. Besana, S. Cadeo, T. Marangon, R. Morandi, R. Piva, A. Spandre, R. Zonca, A. Modelli, E. Varesi, T. Lowrey, A. Lacaita, G. Casagrande, P. Cappelletti and R. Bez. *Novel micro-trench phase-change memory cell for embedded and stand-alone non-volatile memory applications*. In VLSI Technology, 2004. Digest of Technical Papers. 2004 Symposium on, pages 18–19, June 2004. (Cited on page 27.)
- [Pirovano 2003] A. Pirovano, A.L. Lacaita, A. Benvenuti, F. Pellizzer, S. Hudgens and R. Bez. *Scaling analysis of phase-change memory technology*. In Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International, pages 29.6.1–29.6.4, Dec 2003. (Cited on page 21.)
- [Pirovano 2004] A. Pirovano, A. Redaelli, F. Pellizzer, F. Ottogalli, M. Tosi, D. Ielmini, A.L. Lacaita and R. Bez. *Reliability study of phase-change non-volatile memories*. Device and Materials Reliability, IEEE Transactions on, vol. 4, no. 3, pages 422–427, Sept 2004. (Cited on page 24.)
- [Pirovano 2007] A. Pirovano, F. Pellizzer, I. Tortorelli, R. Harrigan, M. Magistretti, P. Petruzza, E. Varesi, D. Erbetta, T. Marangon, F. Bedeschi, R. Fackenthal, G. Atwood and R. Bez. *Self-aligned micro-Trench phase-change memory cell architecture for 90nm technology and beyond*. In Solid State Device Research Conference, 2007. ESSDERC 2007. 37th European, pages 222–225, Sept 2007. (Cited on page 27.)
- [Purvis 2006] Gail Purvis. *Chalcogenides amass off-stage*. III-Vs Review, vol. 19, no. 8, pages 39 – 41, 2006. (Cited on page 17.)
- [Raoux 2008] S. Raoux, G.W. Burr, M.J. Breitwisch, C.T. Rettner, Y.C. Chen, R.M. Shelby, M. Salinga, D. Krebs, S.-H. Chen, H.L. Lung and C.H. Lam. *Phase-change random access memory: A scalable technology*. IBM Journal of Research and Development, vol. 52, no. 4.5, pages 465–479, July 2008. (Cited on pages 25 and 26.)
- [Redaelli 2005] A. Redaelli, D. Ielmini, A.L. Lacaita, F. Pellizzer, A. Pirovano and R. Bez. *Impact of crystallization statistics on data retention for phase change*

- memories*. In Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International, pages 742–745, Dec 2005. (Cited on pages 34 and 35.)
- [Samsung 2005] Samsung. *Memory Technology and Solutions Roadmap*, 2005. "<http://www.samsung.com/>". (Cited on page 17.)
- [Servalli 2009] G. Servalli. *A 45nm generation Phase Change Memory technology*. In Electron Devices Meeting (IEDM), 2009 IEEE International, pages 1–4, Dec 2009. (Cited on pages 23, 27 and 28.)
- [Shin 2011] Sangwoo Shin, Kyung Min Kim, Jiwoon Song, Hyung Keun Kim, Doo Jin Choi and Hyung Hee Cho. *Thermal Stress Analysis of Ge1Sb4Te7 Based Phase-Change Memory Devices*. Electron Devices, IEEE Transactions on, vol. 58, no. 3, pages 782–791, March 2011. (Cited on page 49.)
- [Statistics 2013] World Semiconductor Trade Statistics. *Worldwide semiconductor industry revenue*, 2013. "<https://www.wsts.org/>". (Cited on page 3.)
- [Strenz 2011] R. Strenz. *Embedded Flash technologies and their applications: Status and outlook*. In Electron Devices Meeting (IEDM), 2011 IEEE International, pages 9.4.1–9.4.4, Dec 2011. (Cited on page 10.)
- [Strenz 2014] Strenz. *Embedded NVM for future technology nodes*, 2014. Leti Memory Workshop. (Cited on page 8.)
- [Tanaka 2007] H. Tanaka, M. Kido, K. Yahashi, M. Oomura, R. Katsumata, M. Kito, Y. Fukuzumi, M. Sato, Y. Nagata, Y. Matsuoka, Y. Iwata, H. Aochi and A. Nitayama. *Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory*. In VLSI Technology, 2007 IEEE Symposium on, pages 14–15, June 2007. (Cited on page 10.)
- [Terao 2009] Motoyasu Terao, Takahiro Morikawa and Takeo Ohta. *Electrical Phase-Change Memory: Fundamentals and State of the Art*. Japanese Journal of Applied Physics, vol. 48, no. 8R, page 080001, 2009. (Cited on pages 19 and 21.)
- [Tortorelli 2015] Tortorelli. *Memory market overview and future PCM opportunities*, 2015. Leti Memory Workshop. (Cited on pages 7 and 14.)
- [Turing 1937] A. M. Turing. *On Computable Numbers, with an Application to the Entscheidungsproblem*. Proceedings of the London Mathematical Society, vol. s2-42, no. 1, pages 230–265, 1937. (Cited on pages 1 and 14.)
- [Turing 1947] Alan M Turing. *Lecture to the London Mathematical Society on 20 February 1947*. MD Computing, vol. 12, pages 390–390, 1947. (Cited on page 14.)
- [Utaut 1997] M. Utaut. *Focused Ion Beams*, 1997. (Cited on page 97.)

- [Waser 2009] Rainer Waser, Regina Dittmann, Georgi Staikov and Kristof Szot. *Redox-Based Resistive Switching Memories - Nanoionic Mechanisms, Prospects, and Challenges*. Advanced Materials, vol. 21, pages 2632–2663, 2009. (Cited on page 13.)
- [Williams 2009] David B. Williams and C. Barry Carter. Transmission electron microscopy, a textbook for materials science. Springer, 2009. (Cited on page 101.)
- [Wong 2010] H.-S.P. Wong, S. Raoux, SangBum Kim, Jiale Liang, John P. Reifenberg, B. Rajendran, Mehdi Asheghi and Kenneth E. Goodson. *Phase Change Memory*. Proceedings of the IEEE, vol. 98, no. 12, pages 2201–2227, Dec 2010. (Cited on page 20.)
- [Wright 2006] C.D. Wright, M. Armand and Mustafa M. Aziz. *Terabit-per-square-inch data storage using phase-change media and scanning electrical nanoprobes*. Nanotechnology, IEEE Transactions on, vol. 5, no. 1, pages 50–61, Jan 2006. (Cited on page 112.)

Electrical characterization & TEM Study of the Physical Mechanisms implied in Reliability Issues of Ge-rich GST Phase-Change Memories.

Abstract: In this thesis we provide a detailed study of the mechanisms responsible for data loss in Ge-rich $\text{Ge}_2\text{Sb}_2\text{Te}_5$ Phase-Change Memories, namely resistance drift over time and recrystallization of the amorphous phase. The context of this work is first presented with a rapid overview of the semiconductor memory market and a comparison of emerging non-volatile memories. The working principles of PRAM technology are introduced, together with its advantages, its drawbacks, and the physics governing the crystallization process in phase-change materials, before describing the reliability issues in which we are interested.

A full electrical characterization of devices integrating germanium-enriched GST alloys is then proposed, starting with the characterization of the materials used in our PCM cells and introducing the benefits of Ge-rich GST alloys over standard GST. The electrical performances of devices integrating those materials are analyzed, with a statistical study of the SET & RESET characteristics, programming window, endurance and crystallization speed. We then focus on the main topic of this thesis by analyzing the resistance drift of the SET state of our Ge-rich devices, as well as the retention performances of the RESET state.

In the last part, we investigate on the physical mechanisms involved in these phenomena by providing a detailed study of the cells' structure, thanks to Transmission Electron Microscopy (TEM). The experimental conditions and setups are described before presenting the results which allowed us to go deeper into the comprehension of the resistance drift and the recrystallization of the amorphous phase in Ge-rich devices. A discussion is finally proposed, linking the results of the electrical characterizations with the TEM analyses, leading to new perspectives for the optimization of PRAM devices.

Keywords: Phase-Change Memory (PCM), Ge-rich, reliability, drift, data retention, Transmission Electron Microscopy (TEM).

Caractérisation électrique & analyse TEM des mécanismes physiques impliqués dans les problèmes de fiabilité des mémoires à changement de phase enrichies en germanium.

Résumé: Dans cette thèse, nous proposons une étude détaillée des mécanismes responsables de la perte de données dans les mémoires à changement de phase enrichies en germanium (Ge-rich PRAMs), à savoir la dérive de la résistance au cours du temps et la recristallisation de la phase amorphe. Nous commençons par une présentation du contexte dans lequel s'inscrit cette étude en donnant un aperçu rapide du marché des mémoires à semiconducteur et une comparaison des mémoires non volatiles émergentes. Les principes de fonctionnement de la technologie PRAM sont introduits, avec ses avantages, ses inconvénients, ainsi que la physique régissant le processus de cristallisation dans les matériaux à changement de phase, avant de décrire les problèmes de fiabilité qui nous intéressent.

Une caractérisation électrique complète de dispositifs intégrant des alliages de GST enrichi en germanium est ensuite proposée, en commençant par la caractérisation des matériaux utilisés dans nos cellules, introduisant alors les avantages des alliages enrichis en Ge sur le GST standard. Les performances électriques des dispositifs intégrant ces matériaux sont analysées, avec une étude statistique des caractéristiques SET & RESET, de la fenêtre de programmation, de l'endurance et de la vitesse de cristallisation. Nous nous concentrons ensuite sur le thème principal de cette thèse en analysant la dérive en résistance de l'état SET de nos dispositifs Ge-rich, ainsi que les performances de rétention de l'état RESET.

Dans la dernière partie, nous étudions les mécanismes physiques impliqués dans ces phénomènes en fournissant une étude détaillée de la structure des cellules, grâce à l'utilisation de la Microscopie Electronique en Transmission (MET). Les conditions et configurations expérimentales sont décrites, avant de présenter les résultats qui nous ont permis d'aller plus loin dans la compréhension de la dérive en résistance et de la recristallisation de la phase amorphe dans les dispositifs Ge-rich. Une discussion est finalement proposée, reliant les résultats des caractérisations électriques avec ceux des analyses TEM, conduisant à de nouvelles perspectives pour l'optimisation des dispositifs PRAMs.

Mots clés : Mémoires à changement de phase, Ge-rich, fiabilité, drift, rétention de donnée, Microscopie Electronique en Transmission.

Résumé français

I. Introduction

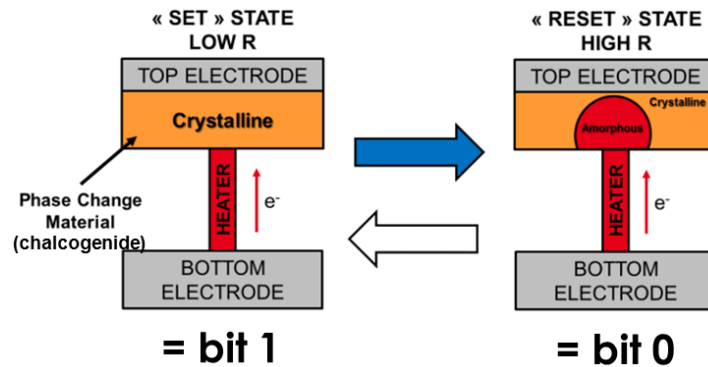


Fig. 1 : principe de fonctionnement d'une mémoire à changement de phase. Le stockage de l'information repose sur le basculement du matériau entre une phase amorphe (état hautement résistif, dit « RESET ») et une phase cristalline (état faiblement résistif, dit « SET »), rendu possible par le chauffage du matériau à changement de phase grâce à l'application de pulses électriques.

Depuis l'invention des premiers ordinateurs électroniques dans les années 30, l'importance des mémoires dans notre vie quotidienne n'a cessé de croître. Elles sont présentes de nos jours dans la plupart des systèmes électroniques comme les ordinateurs, les téléphones portables, les télévisions, l'électroménager, les consoles de jeux... Si la technologie Flash dominait le marché des mémoires non-volatiles jusqu'à maintenant, ses limitations physiques l'empêchent d'atteindre des niveaux de miniaturisation plus critiques, et ouvrent de ce fait la voie à de nouvelles technologies comme les mémoires à changement de phase (ou PCM pour "Phase-Change Memories", fig. 1), souvent considérées comme l'alternative la plus prometteuse. En effet la structure et le principe de fonctionnement de ces dernières offrent de nombreux avantages, notamment un fort potentiel de miniaturisation, des vitesses d'écriture élevées, une grande endurance et un faible coût de production. Cependant, certains points clés concernant la fiabilité des PCM doivent encore être améliorés afin de pouvoir répondre au cahier des charges d'applications contraignantes comme le marché automobile, où les mémoires sont soumises à de hautes températures. Au cours de ces dernières années, de nombreux efforts ont été faits pour améliorer la stabilité thermique des PCMs, et de remarquables progrès ont été accomplis dans ce sens avec le développement de matériaux innovants tels que les alliages de $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) enrichis en germanium, ou "Ge-rich GST". Malheureusement, l'utilisation de ces matériaux accentue un autre phénomène nuisible à la fiabilité des mémoires : la dérive de la résistance au fil du temps, ou « drift » (fig. 2). Dans cette thèse, les mécanismes physiques régissant la fiabilité des PCM enrichies en germanium sont étudiés, d'abord par la caractérisation des performances électriques des mémoires, puis en couplant ces résultats avec les analyses morphologiques obtenues par Microscopie Electronique en Transmission (MET ou TEM pour "Transmission Electron Microscopy"). Ce couplage systématique entre analyses électriques et morphologiques des dispositifs nous permettra ainsi d'apporter des éléments de réponse quant aux mécanismes microscopiques à l'origine des phénomènes étudiés.

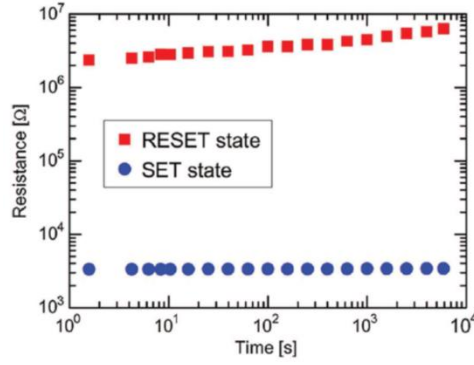


Fig. 2 : illustration du drift de la résistance des mémoires PCM au cours du temps (Boniardi et al., IEEE 2010).

II. Caractérisations électriques

Afin d'évaluer le comportement des matériaux étudiés en fonction de la température, plusieurs types de caractérisations ont été effectuées sur des couches minces d'alliages de GST enrichis avec différents pourcentage de germanium. En premier lieu, la température de cristallisation de ces alliages a été déterminée par mesure de la résistivité du matériau en fonction de la température. Les résultats de ces expériences (fig. 3) montrent que l'enrichissement en germanium permet d'augmenter considérablement la température de cristallisation des matériaux, améliorant de ce fait leur stabilité thermique.

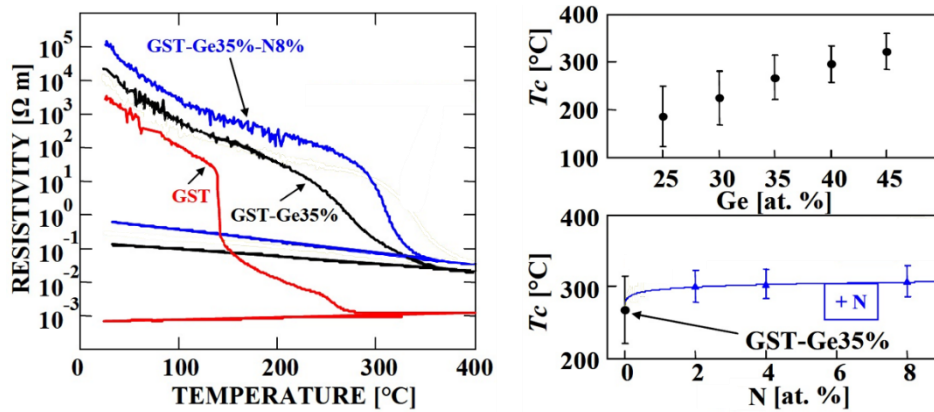


Fig. 3 : mesures de résistivité des matériaux étudiés en fonction de la température. La chute soudaine de la résistivité correspond à la cristallisation du matériau. Les températures de cristallisation ainsi mesurées augmentent avec le pourcentage de germanium présent dans le matériau. Le dopage en azote participe également à cette augmentation.

Ces matériaux ont ensuite été intégrés dans des mémoires de type « wall » (fig. 4) afin de tester leurs performances électriques. Si les tests de rétention de données ont montré que l'enrichissement en germanium permettait de garder l'information stockée pendant 10 ans à plus de 200°C (contre 85°C pour le GST standard), les mesures de drift ont en revanche révélé que cet enrichissement tend également à accentuer la dérive de la résistance au cours du temps (fig. 5). Ce phénomène étant préjudiciable à la fiabilité des états SET de ces mémoires, d'autres méthodes de programmation ont été testées (fig. 6), en mesurant également leur impact sur le drift des mémoires (fig. 7). La programmation SETMIN, correspondant à une série

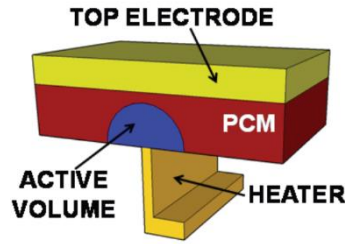


Fig. 4 : schéma de la structure des mémoires étudiées. Les impulsions électriques sont appliquées au matériau à changement de phase par le biais du « heater ». La zone active désigne alors le volume de matériau affecté par les impulsions.

d'impulsions électroniques d'intensité décroissante, permet d'atteindre les plus faibles coefficients de drift mesurés, mais présente l'inconvénient d'être beaucoup trop longue pour des applications industrielles. La programmation dite SETLOW, correspondant à une impulsion RESET suivie quelques nanosecondes plus tard d'une impulsion SET, permet d'atteindre des états faiblement résistifs en utilisant des courants plus faibles qu'une programmation SET standard, et d'obtenir des coefficients de drift proches de ceux obtenus par la programmation SETMIN, tout en maintenant des temps de programmation acceptables.

La structure du matériau à changement de phase à l'intérieur des mémoires ainsi programmées a ensuite été étudiée par microscopie électronique en transmission, dans le but de comprendre les raisons microscopiques à l'origine de ces différences de comportement macroscopiques.

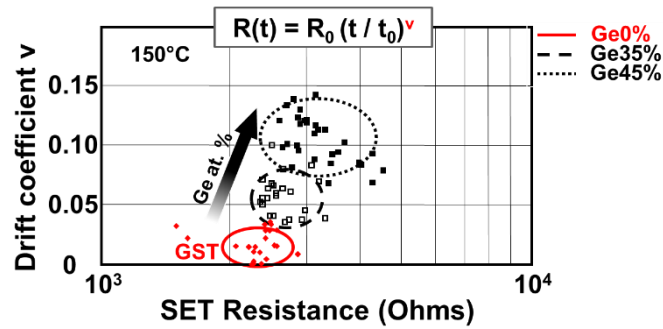


Fig. 5 : coefficients de drift mesurés sur des mémoires Ge-rich, montrant l'augmentation du phénomène de drift avec l'enrichissement en germanium.

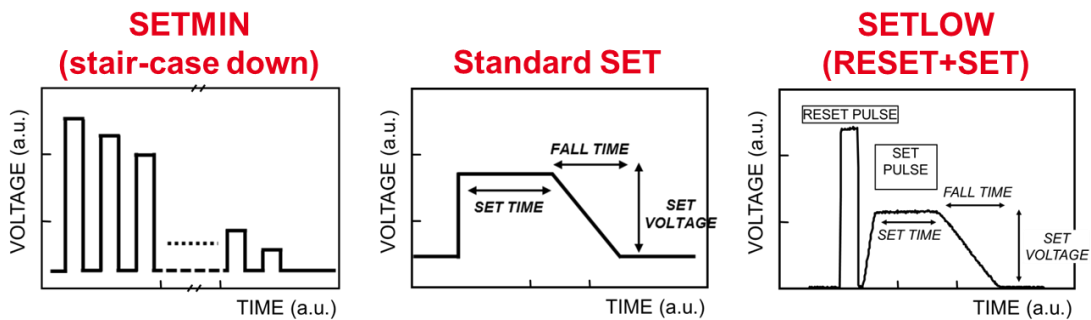


Fig. 6 : les trois procédures de programmation SET étudiées : au centre, la programmation SET standard ; à gauche, la procédure SETMIN ; et à droite, la programmation SETLOW.

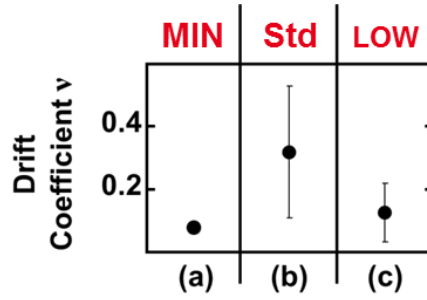


Fig. 7 : moyenne des coefficients de drift mesurés en fonction de l'état de programmation des mémoires. La programmation SETMIN permet d'obtenir les plus faibles coefficients, suivi de la programmation SETLOW qui présentent également des valeurs plus faibles que la programmation SET standard

III. Analyses TEM et simulations

Les résultats des analyses TEM permettent de mettre en évidence les différences morphologiques entre les mémoires programmées dans les états RESET, SET, SETMIN et SETLOW. Comme prévu, les états RESET présentent une zone active amorphe (zone active = région du matériau à changement de phase affectée par les impulsions électroniques), tandis que cette zone est cristalline dans les états SET et SETMIN (fig. 8).

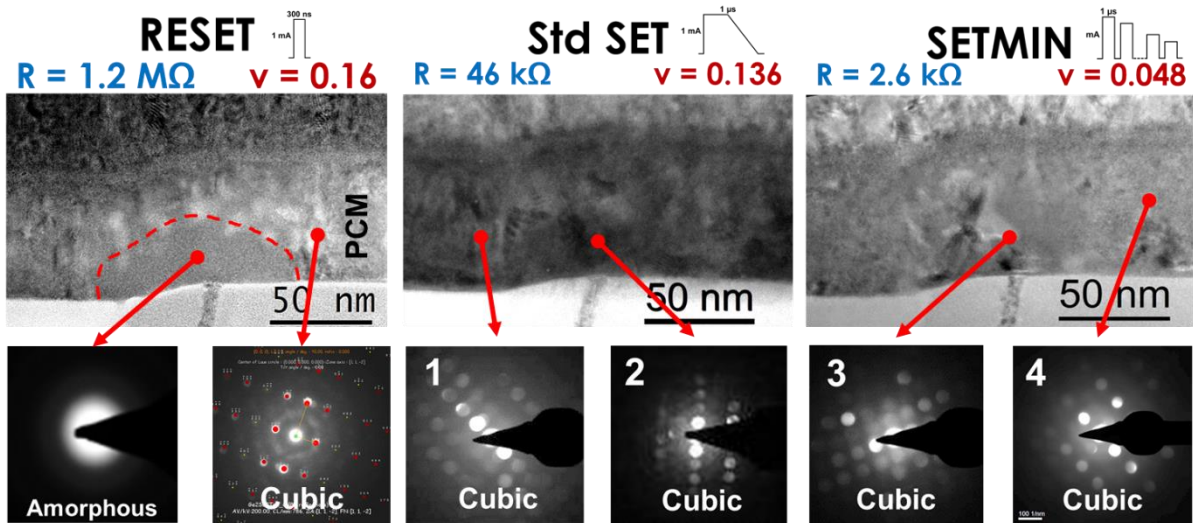


Fig. 8 : images TEM en champ clair et clichés de diffraction obtenus sur trois mémoires en état RESET, SET standard et SETMIN. Le dôme amorphe créé par l'impulsion RESET est bien visible, alors que les états SET et SETMIN présentent une zone active totalement cristalline.

La zone active des mémoires programmées dans l'état SETLOW présente une morphologie particulière, jusqu'alors jamais observée, constituée d'une colonne cristalline traversant un dôme amorphe (fig. 9). Ces différences de structures cristallines sont encore plus visibles sur les images en champ sombre (fig. 10) : la zone active des états SET présentent de nombreux grains cristallins de tailles très inférieures à ceux mis en évidence dans les états SETMIN, dans lesquels on peut observer la formation d'une structure cristalline couvrant toute l'épaisseur du matériau à changement de phase et permettant ainsi une meilleure conduction du courant du heater à la top electrode. Les états SETLOW présentent également une structure cristalline similaire, mais cette dernière est entourée de matériau amorphe, résidus de l'amorphisation

engendrée par l'impulsion RESET. La formation de cette « colonne » cristalline dans les états SETLOW a été étudiée à l'aide de simulations recréant la cristallisation de la zone active à faibles courants (fig. 11). Les résultats de ces simulations montrent la croissance du matériau cristallin au-dessus du dome amorphe jusqu'à atteindre le heater, laissant deux poches de matériau amorphe de part et d'autre du chemin conducteur ainsi créé. Ces résultats concordent avec les observations TEM et permettent d'expliquer comment la programmation SETLOW permet d'atteindre des états très faiblement résistifs.

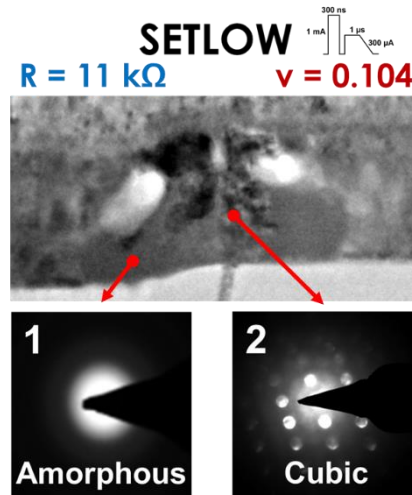


Fig. 9 : images TEM en champ clair et clichés de diffraction obtenus sur une mémoire programmée en état SETLOW, montrant la présence de deux zones, l'une amorphe et l'autre cristalline, à l'intérieur de la zone active.

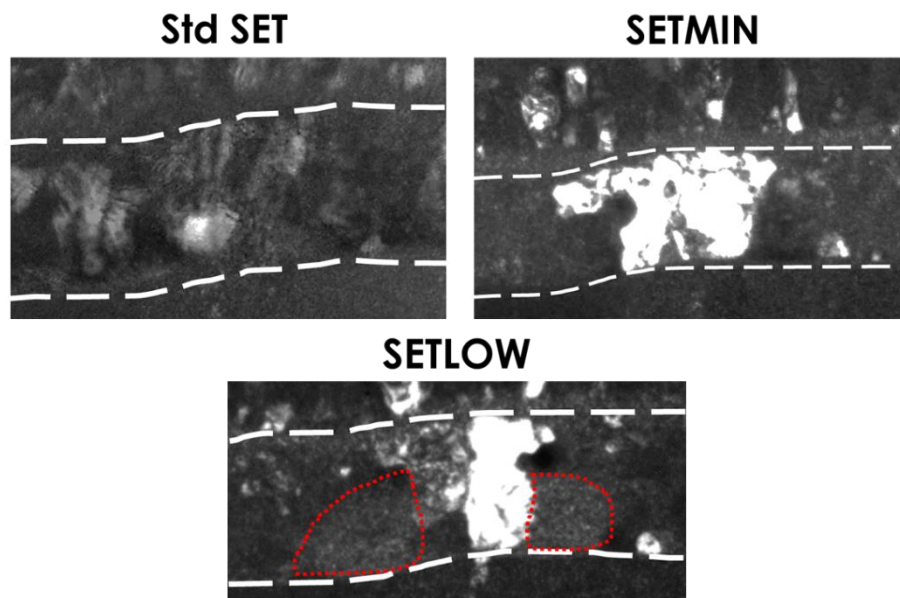


Fig. 10 : images TEM en champ sombre des mémoires programmées en état SET standard, SETMIN et SETLOW. Les états SETMIN et SETLOW présentent de larges structures cristallines s'étendant du heater jusqu'à la top electrode, tandis que des grains cristallins plus petits et plus nombreux sont visibles dans la mémoire SET standard. La morphologie particulière de l'état SETLOW est également mise en évidence, avec un résidu de dôme amorphe traversé par un chemin cristallin.

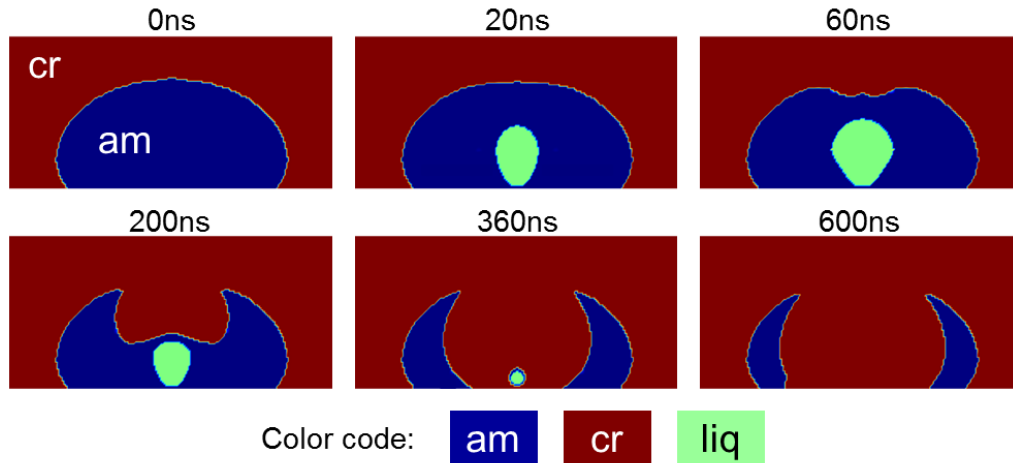


Fig. 11 : résultats des simulations de programmation SET à faible courant (SETLOW), montrant la croissance du cristal au dessus du dôme amorphe vers le heater, laissant deux poches de résidus amorphes de part et d'autre du chemin cristallin ainsi créé.

La migration des atomes à l'intérieur du matériau à changement de phase a également été étudiée par spectroscopie EELS (Electron Energy Loss Spectroscopy). Les cartographies réalisées à l'aide de cette technique permettent de mettre en évidence la répartition des éléments dans le matériau, et en particulier dans la zone active. Les résultats obtenus (fig. 12) montrent la migration des atomes de germanium vers la périphérie de la zone active tandis que le tellure et l'antimoine migrent vers l'intérieur de cette dernière, et ce quelle que soit l'état de programmation des cellules. La concentration en germanium dans la zone active reste cependant bien plus élevée dans les dispositifs enrichis en germanium que dans les mémoires intégrant du GST non enrichi, et c'est pourquoi les cellules Ge-rich présentent une meilleure rétention des données (Cf résultats des caractérisations électriques).

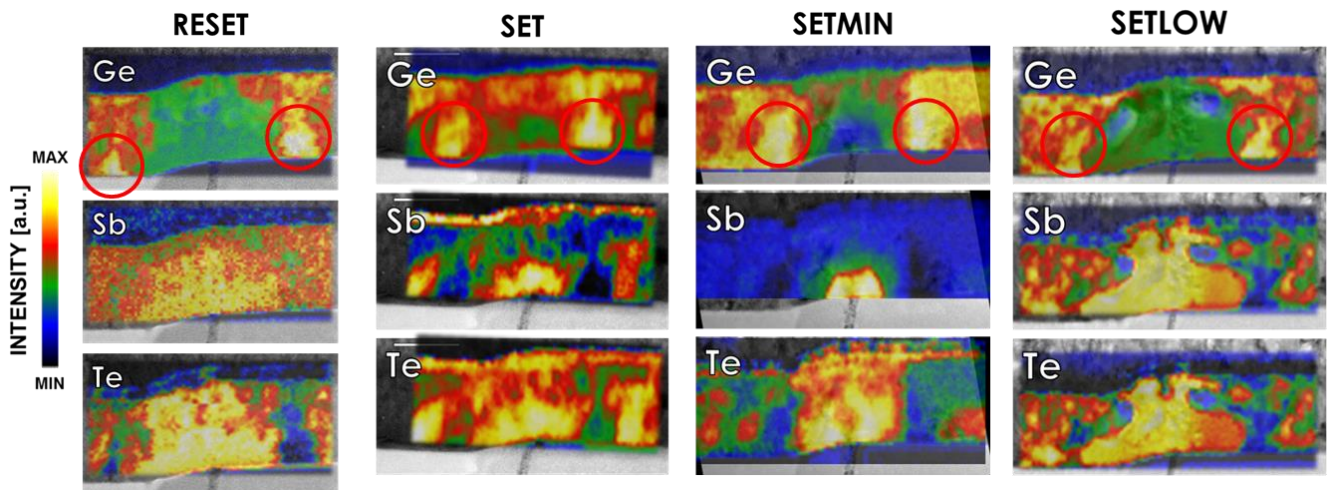


Fig. 11 : cartographies EELS de la répartition des éléments dans les mémoires étudiées, montrant la même tendance de migration atomique en dépit de l'état de programmation : les atomes de germanium tendent à être expulsés vers la périphérie de la zone active tandis que le tellure et l'antimoine s'y concentrent.

IV. Conclusion

Cette étude a permis de répondre à deux principales interrogations :

- Premièrement, comment expliquer et limiter l'augmentation du phénomène de drift dans les états SET des mémoires Ge-rich ?
- Et deuxièmement, comment expliquer les performances de rétention des états RESET de ces mémoires ?

Concernant le phénomène de drift dans les états SET, nous avons vu que le paramétrage des impulsions électriques utilisées pour programmer les cellules permet de minimiser cet effet. Les analyses TEM ont montré que la programmation SETLOW est à l'origine de la création d'un chemin de conduction efficace avec peu de résidus amorphes comparé à la programmation SET standard, conduisant ainsi à un drift réduit.

Pour ce qui est de la rétention des états RESET, les cartographies EELS ont révélé la tendance générale de migration des atomes de germanium qui sont expulsés de la zone active. L'enrichissement en germanium permet cependant de balancer ce phénomène et de garder une composition plus riche en germanium que dans les zones actives des mémoires au GST non enrichi, améliorant ainsi les performances de rétention de données.

Ces résultats permettent d'avancer dans la compréhension des phénomènes physiques régissant les performances électriques des mémoires à changement de phase. Ils participent ainsi à l'optimisation de ces dernières et au développement de nouvelles perspectives, comme l'élaboration de matériaux encore plus efficaces, ou de nouvelles architectures comme la structure confinée, permettant l'essor des mémoires à changement de phases vers de nouveaux marchés potentiels.